A 0.7V Time-based Inductor for Fully Integrated Low Bandwidth Filter Applications

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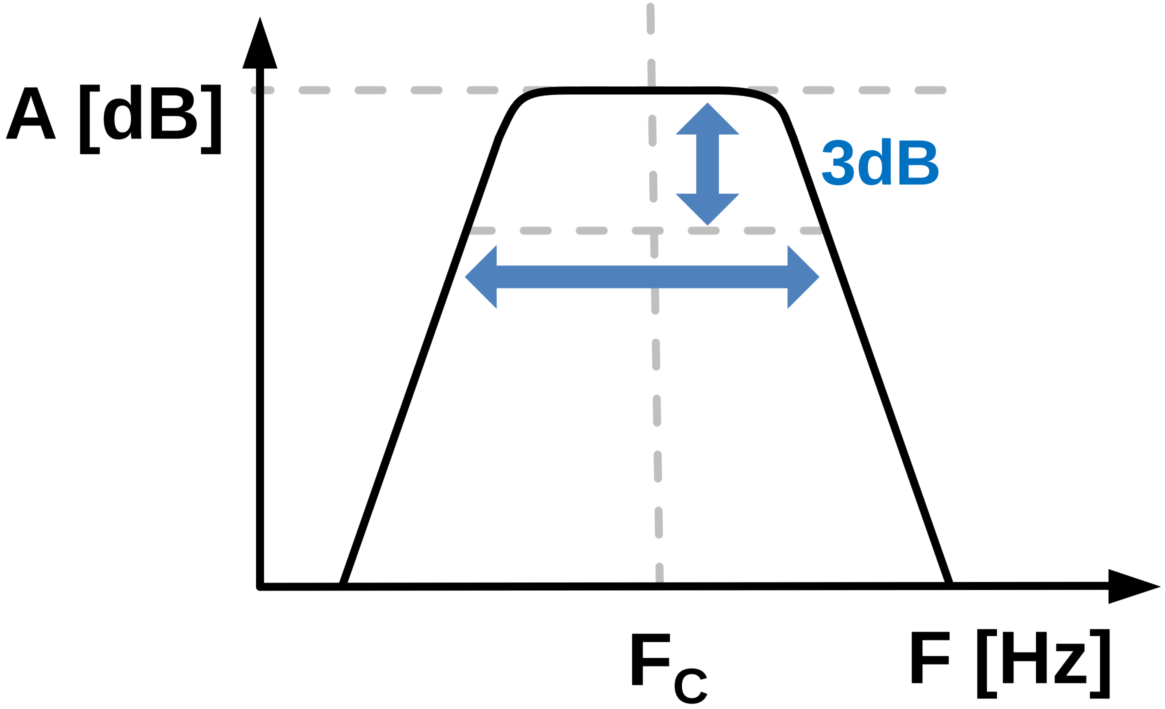
Outline

- **Motivation**
- **Proposed Architecture**
- **Circuit Implementation**
- **Measurement Results**
- **Summary**

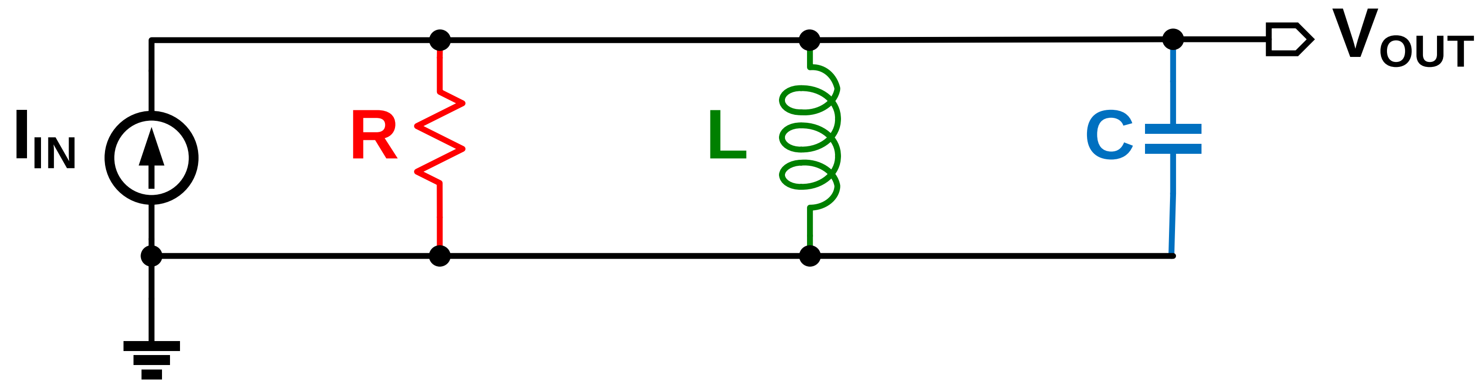
Filter Metrics



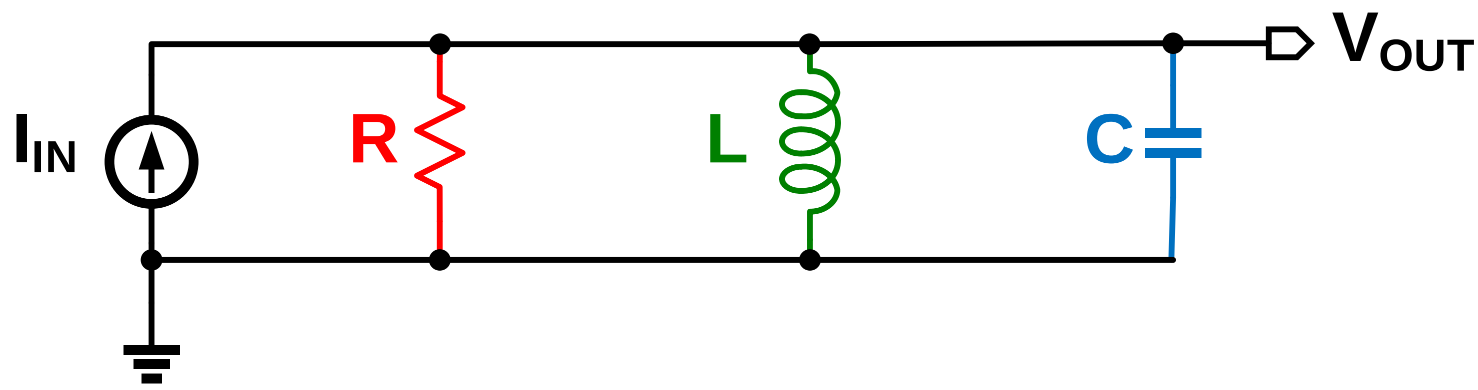
- Frequency
- Gain
- Bandwidth

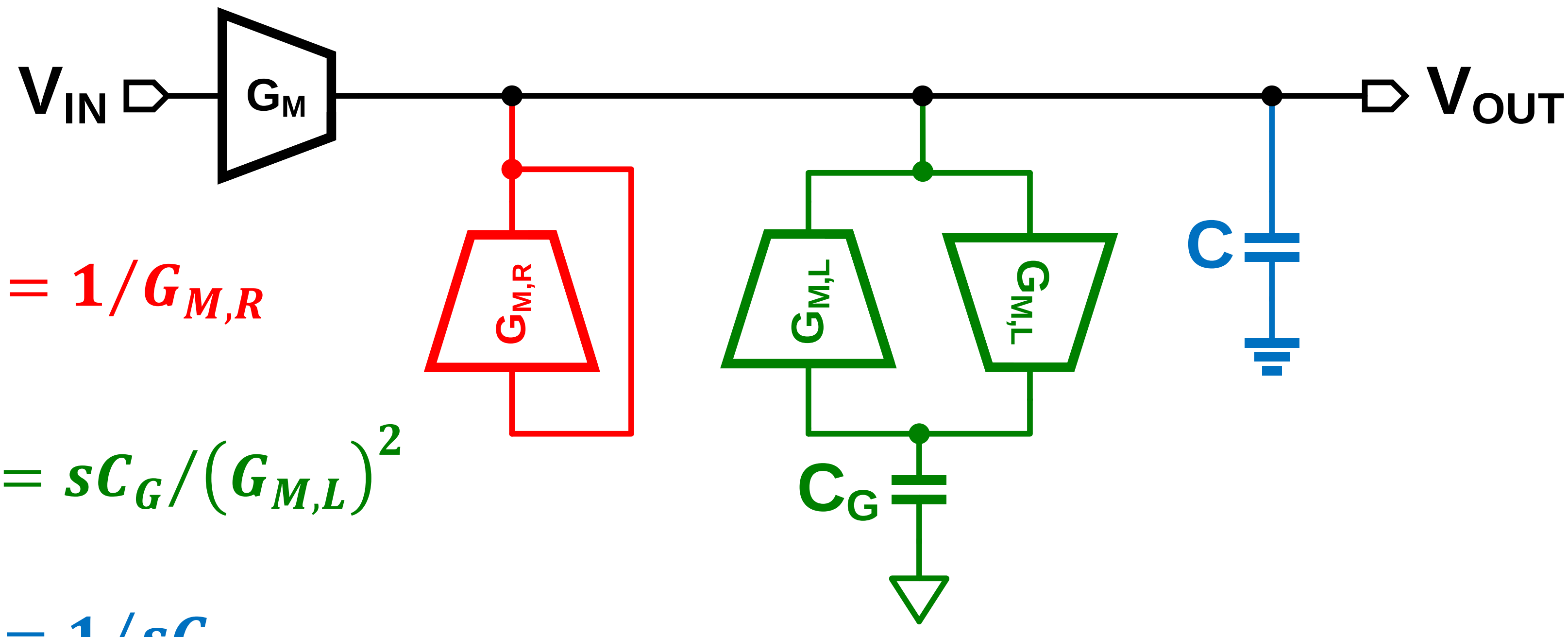
- Power
- DR
- V_{DD}

Bandpass Filter Topology



Bandpass Filter Topology





$$Z_R = 1/G_{M,R}$$

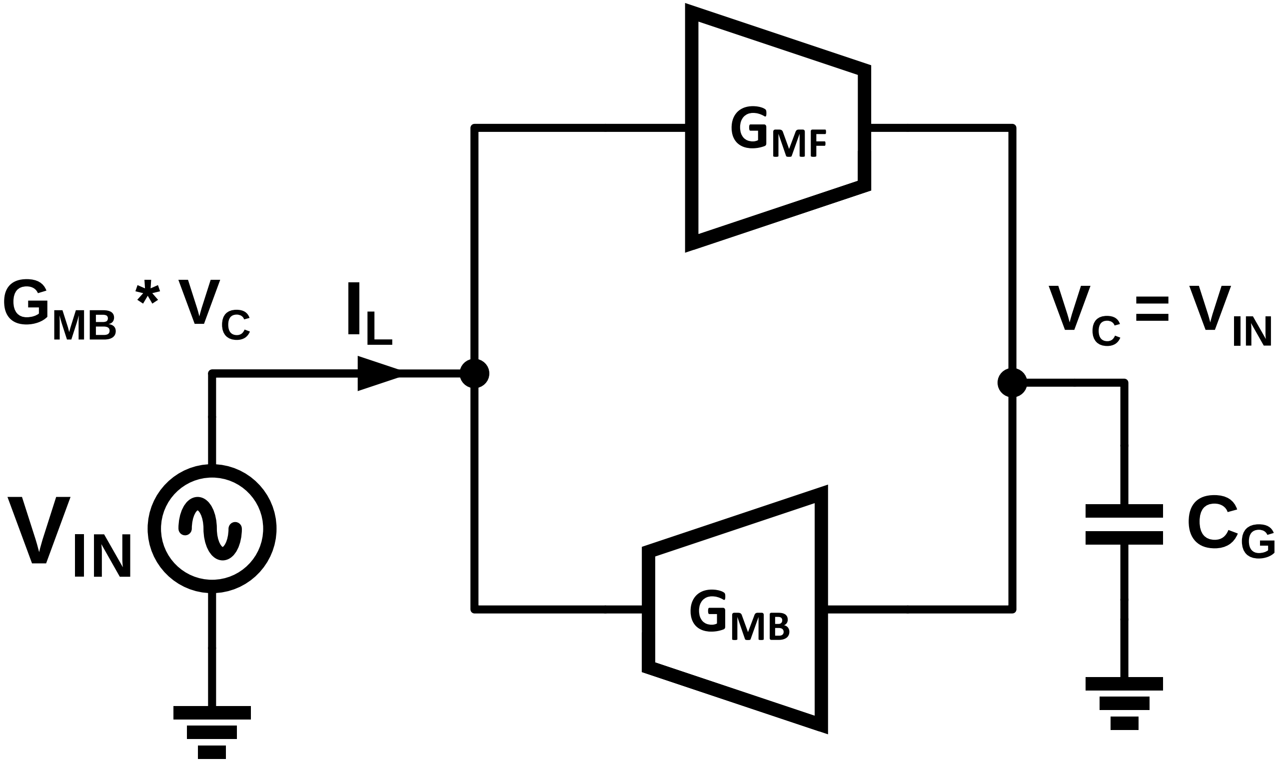
$$Z_L = sC_G/\left(G_{M,L}\right)^2$$

$$Z_C = 1/sC$$

Ideal Gyrator Circuit

$I_L = G_{MB} * V_C$

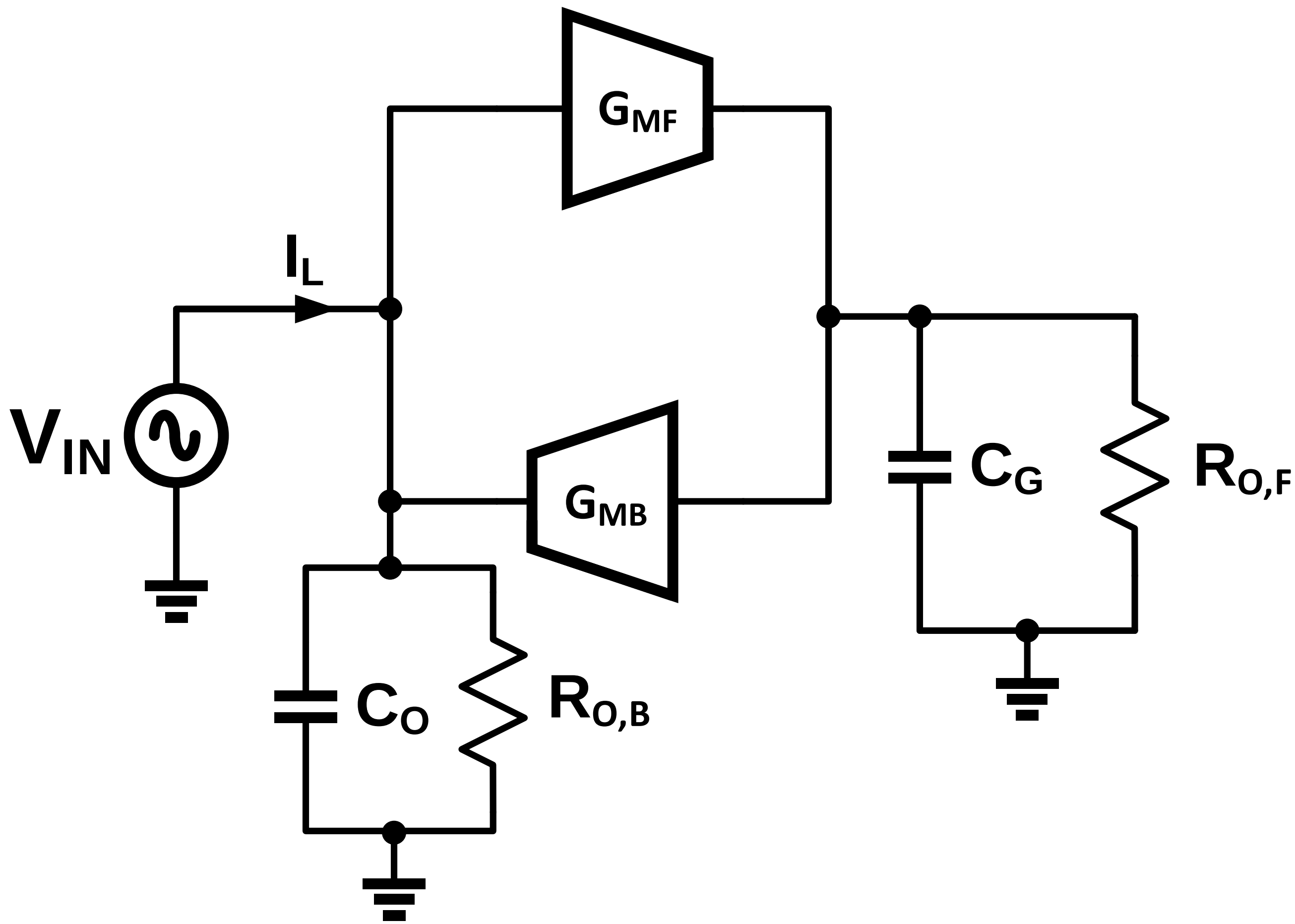
$V_C = V_{IN}\, G_{MF} * 1/sC_G$



$$Z_{IN} = \frac{sC_G}{G_{MB}G_{MF}}$$

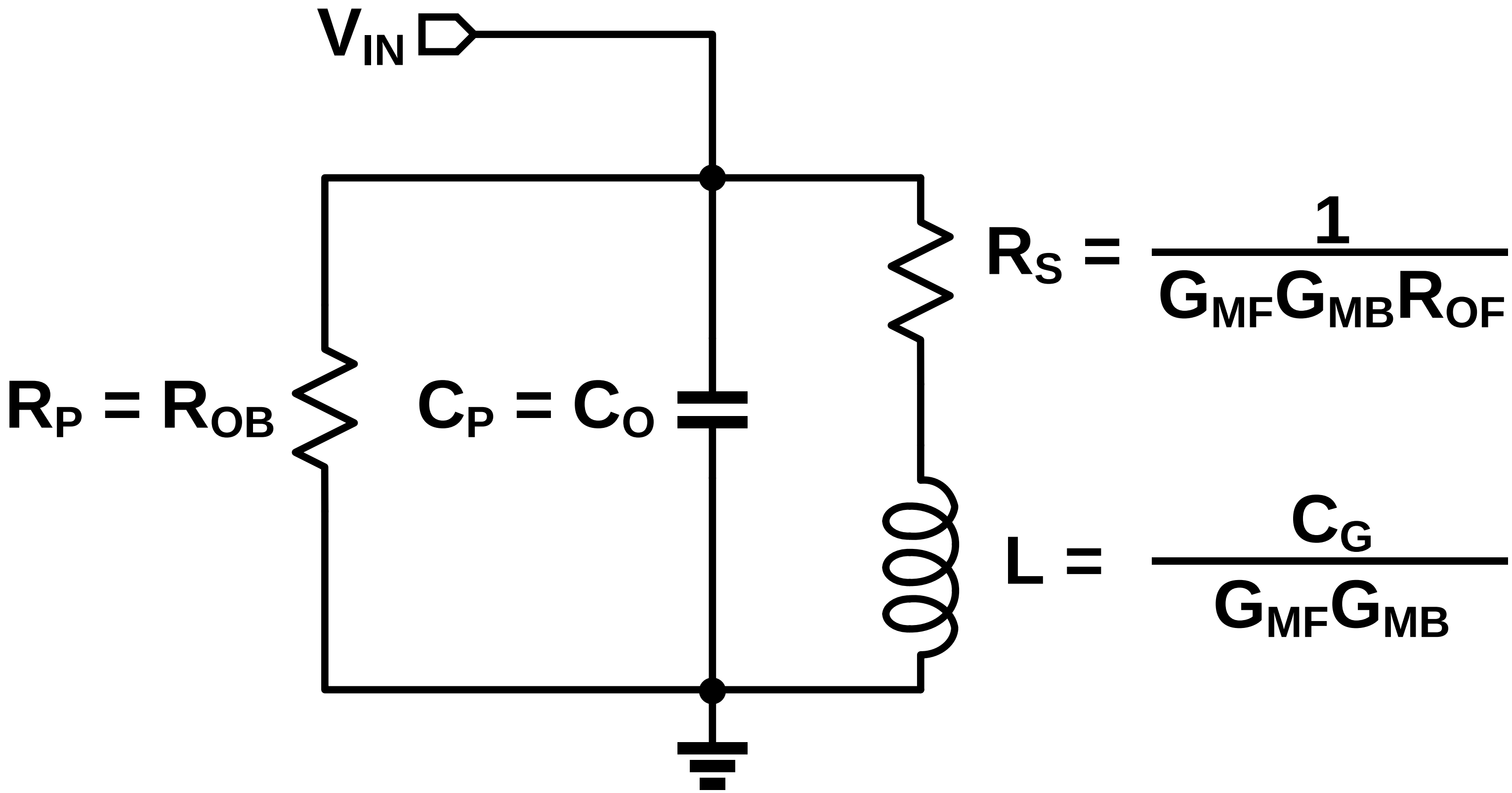
Practical Gyrator

- G_M cells have finite output impedance

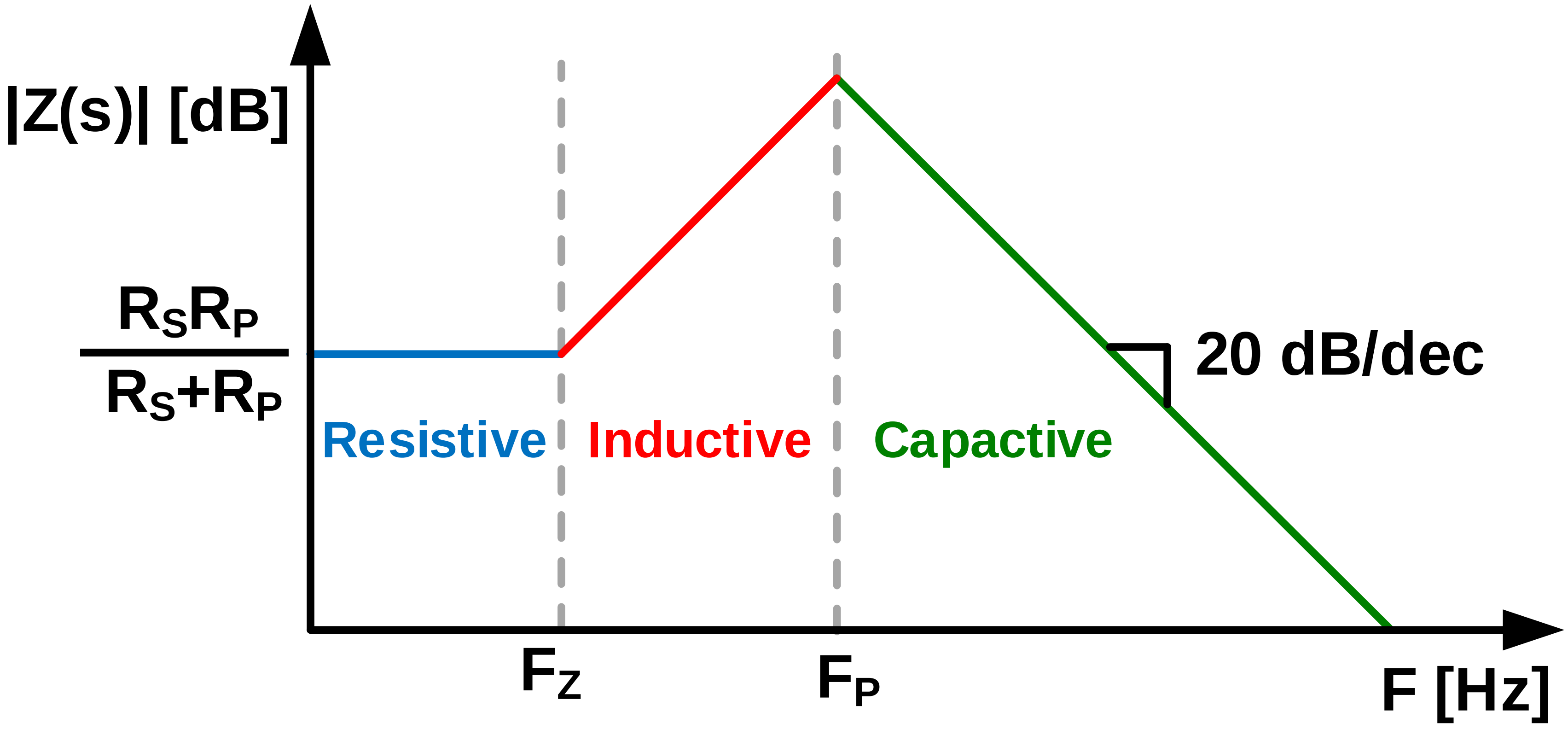


Small Signal Gyrator Model

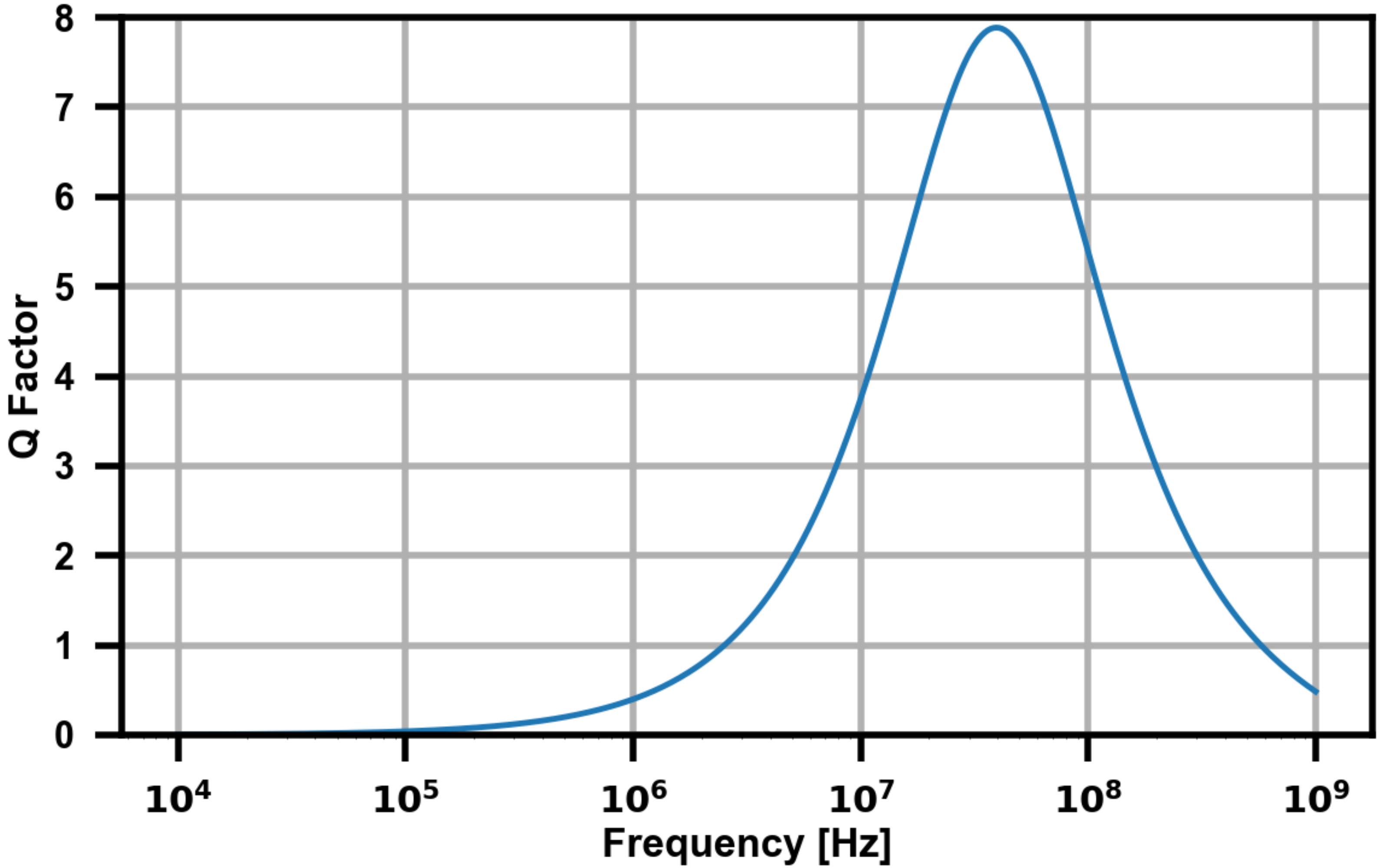
- **Gyrator can be viewed as RLC circuit**



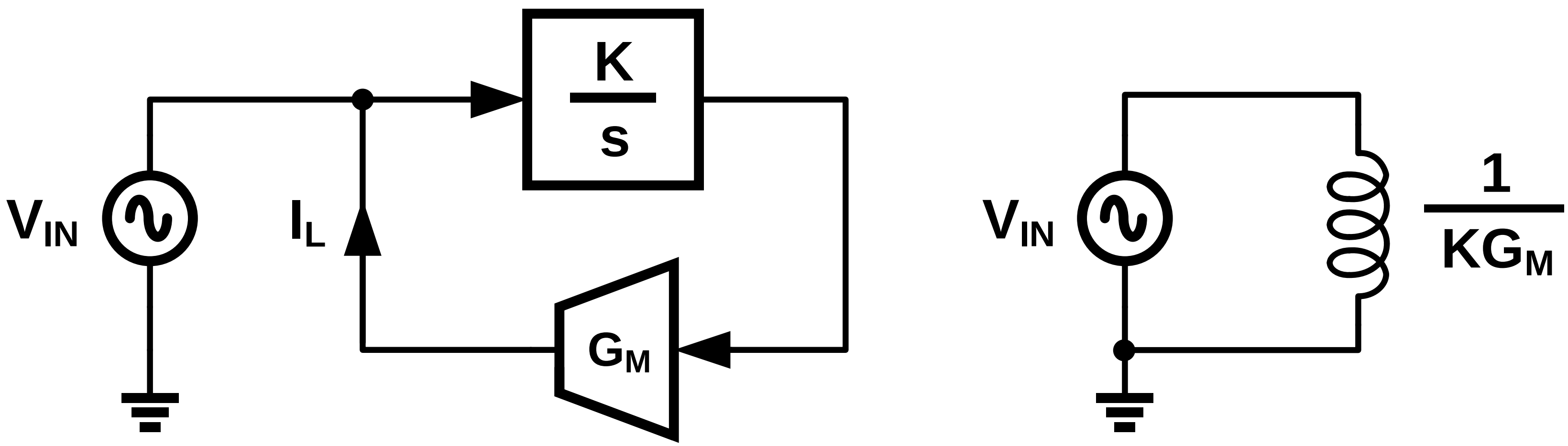
Gyrator Transfer Function



Gyrator Quality Factor



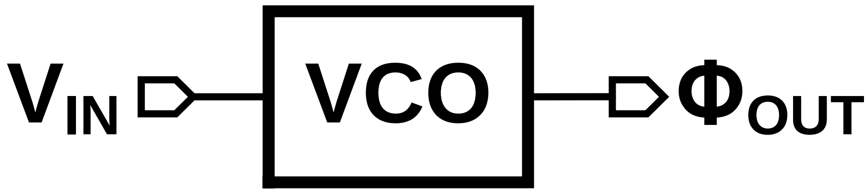
Inductor Modeling



- **L scales inversely with integrator gain**

- **Need a better integrator!**

Time-Based Integrator



$$K_{VCO} = \frac{F_{OUT}}{V_{IN}}$$

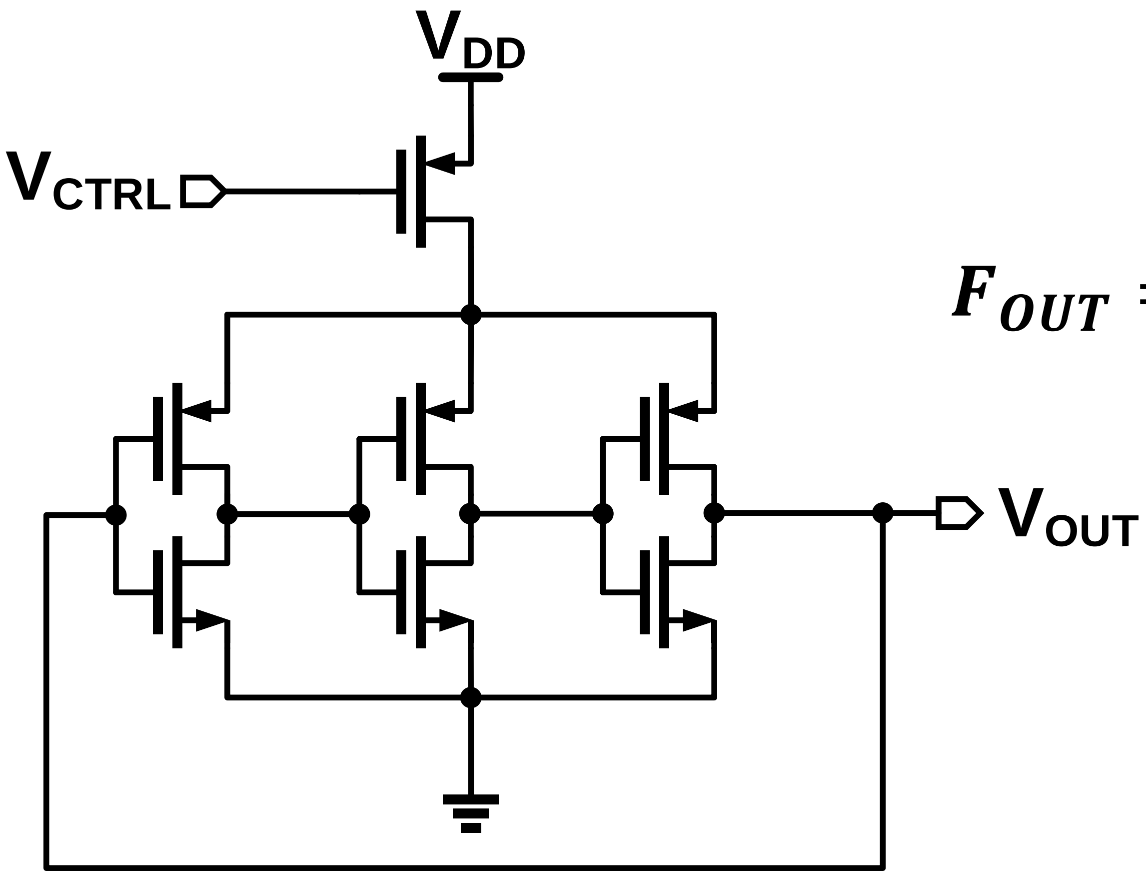
$$F_{OUT} = \frac{\partial \Phi_{OUT}}{\partial t} = s\,\Phi_{OUT}$$

$$H_{VCO}(s) = \frac{\Phi_{OUT}(s)}{V_{IN}(s)} = \frac{K_{VCO}}{s}$$

Oscillator is a V to Φ integrator

Ring Oscillator

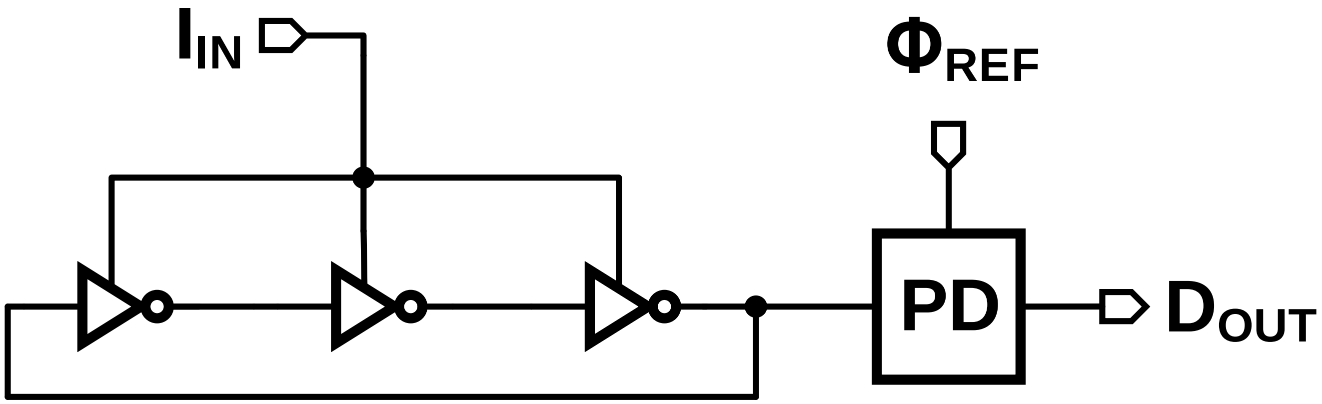
- V_{CTRL} converted to current by PMOS
- Delay cells easily scalable, low area



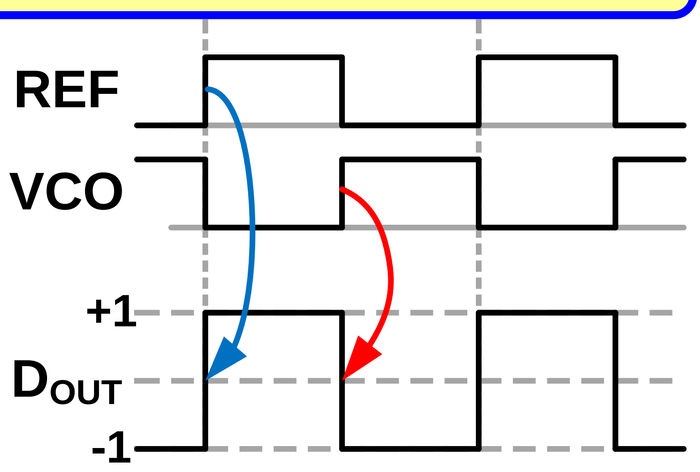
$$F_{OUT} = \frac{1}{2\sum t_p}$$

Back to the Voltage?

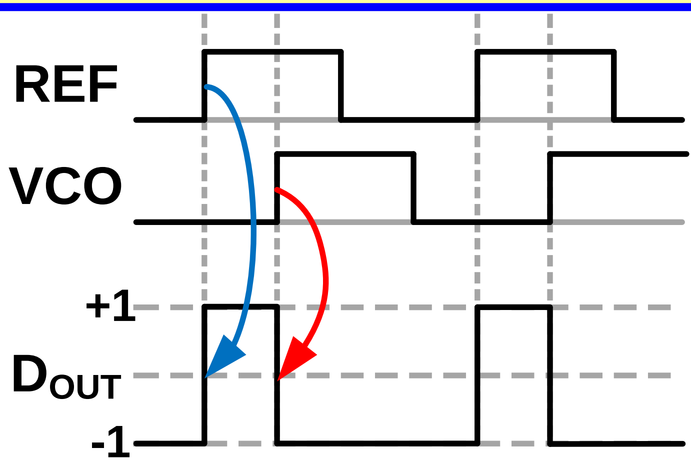
- PD converts input phase to PWM voltage output



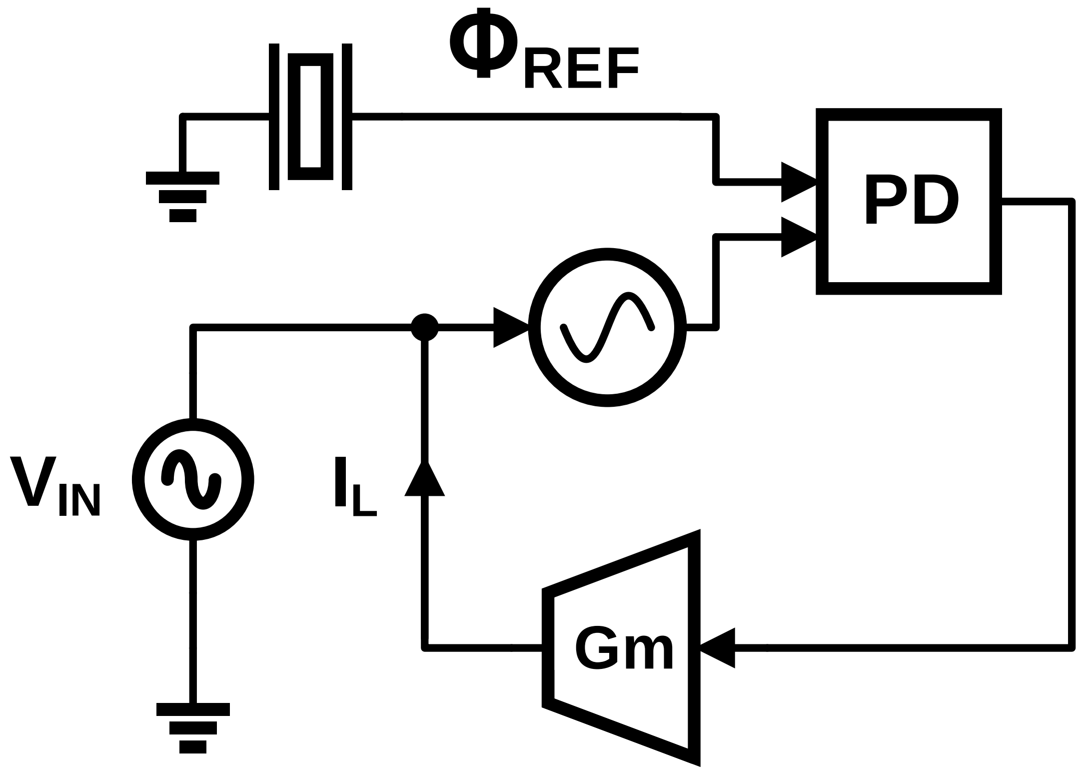
$$\Delta\Phi = \pi \rightarrow D_{OUT} = 0.5$$



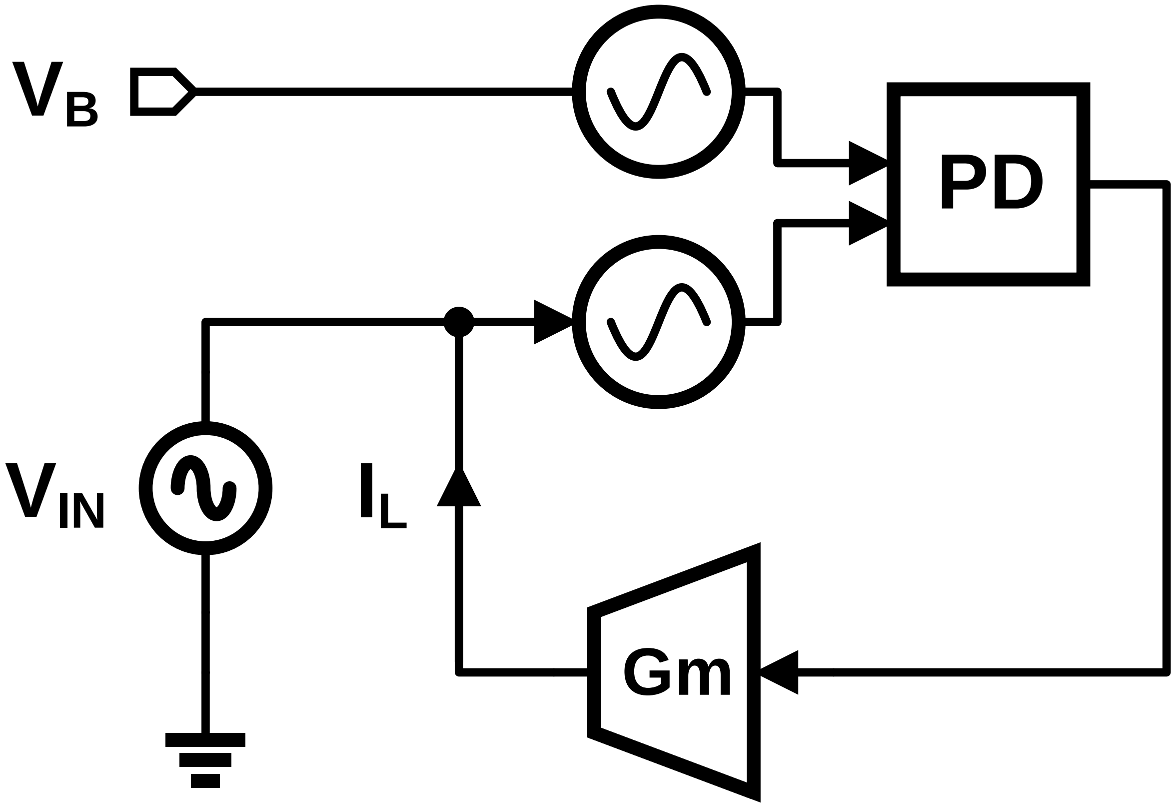
$$\Delta\Phi = \pi/2 \rightarrow D_{OUT} = 0.25$$



Time-Based Inductor



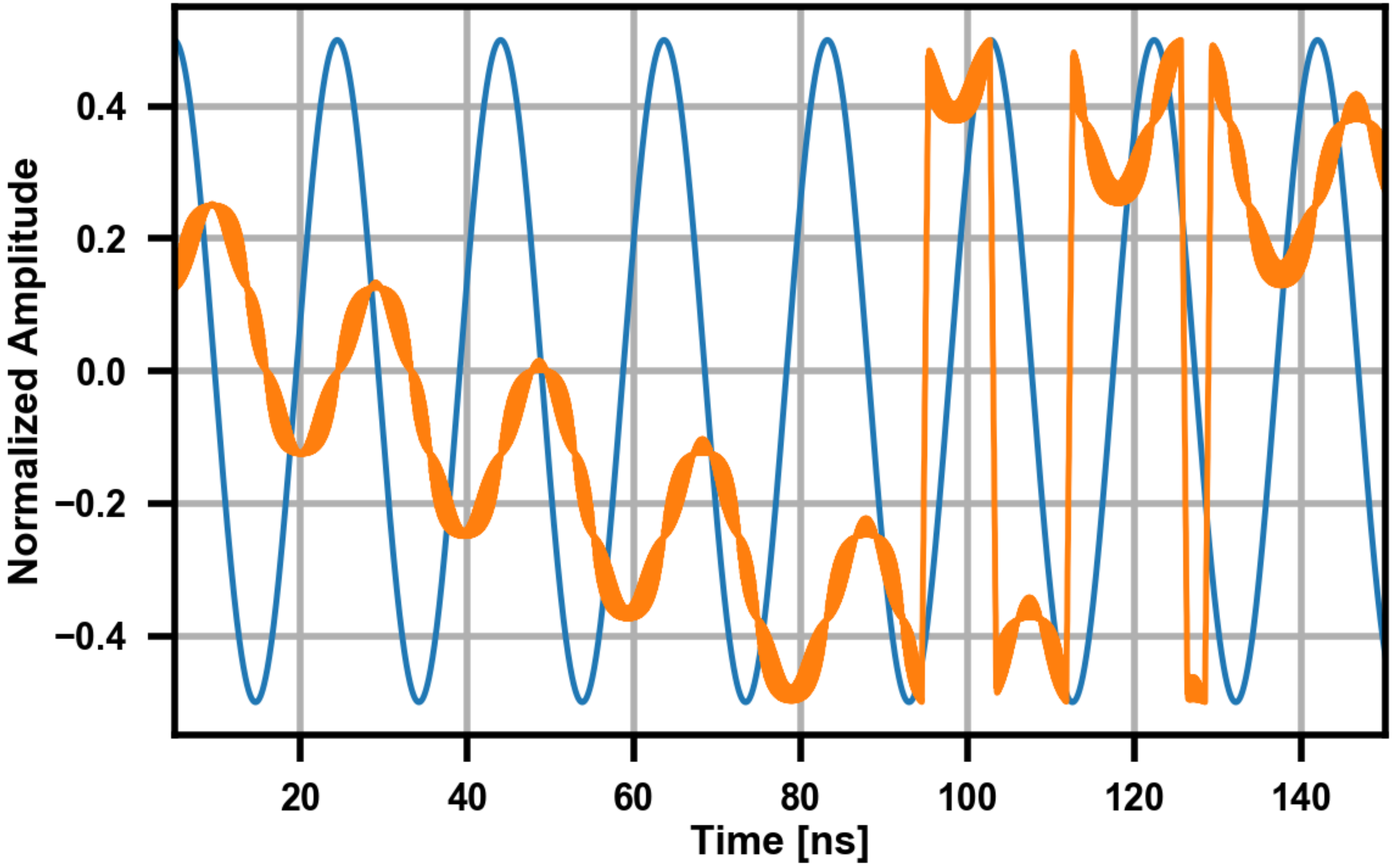
Time-Based Inductor



$$L = \frac{1}{K_{VCO} K_{PD} G_M}$$

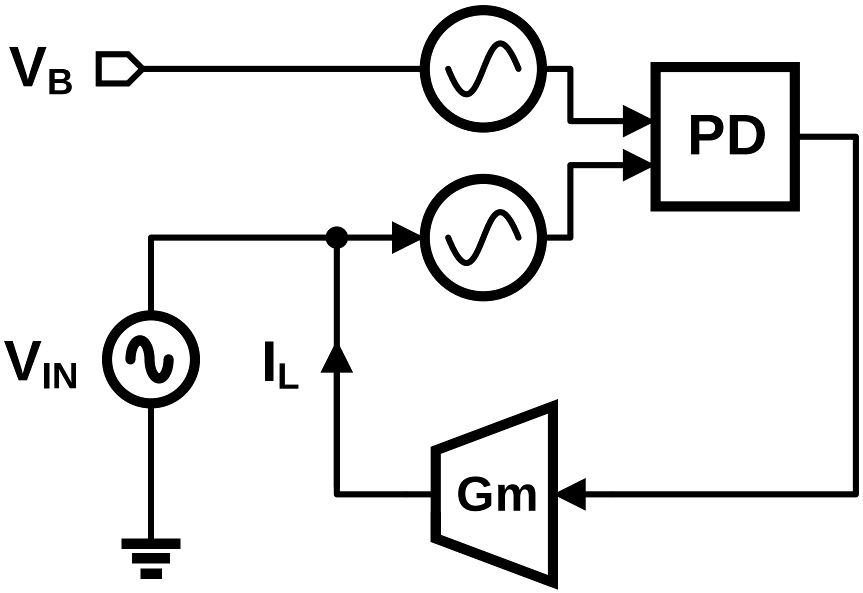
Effect of VCO F_{FR} Mismatch

- **Any offset is continuously integrated**



PD Input Range

- K_{PD} has limited linear input range



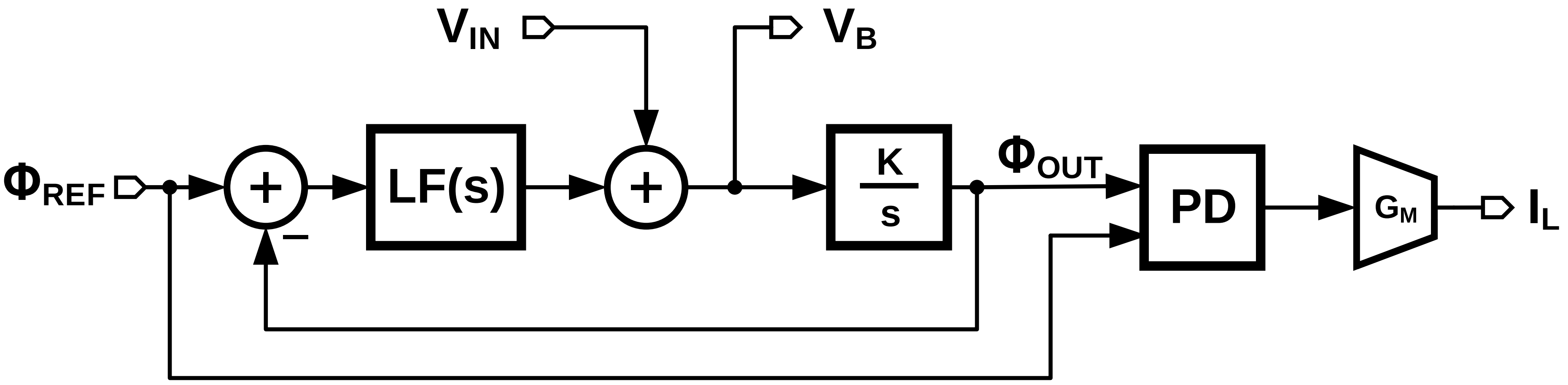
$$V_{IN} = A\sin(\omega_{IN} t)$$

$$\Delta F = A\, K_{VCO}$$

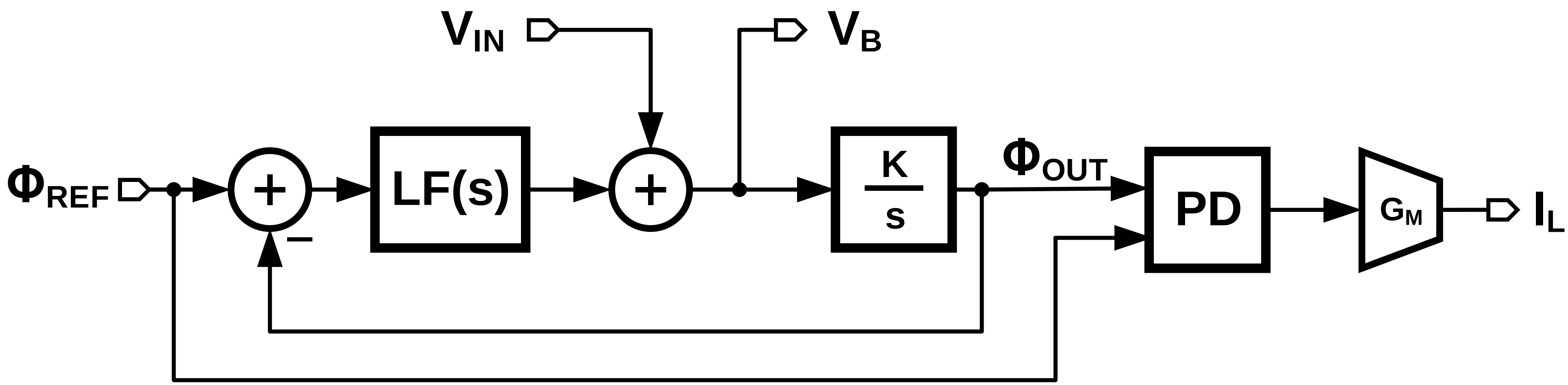
$$\Delta\Phi = \frac{A K_{VCO}}{\omega_{IN}} \leq \Delta\Phi_{Max}$$

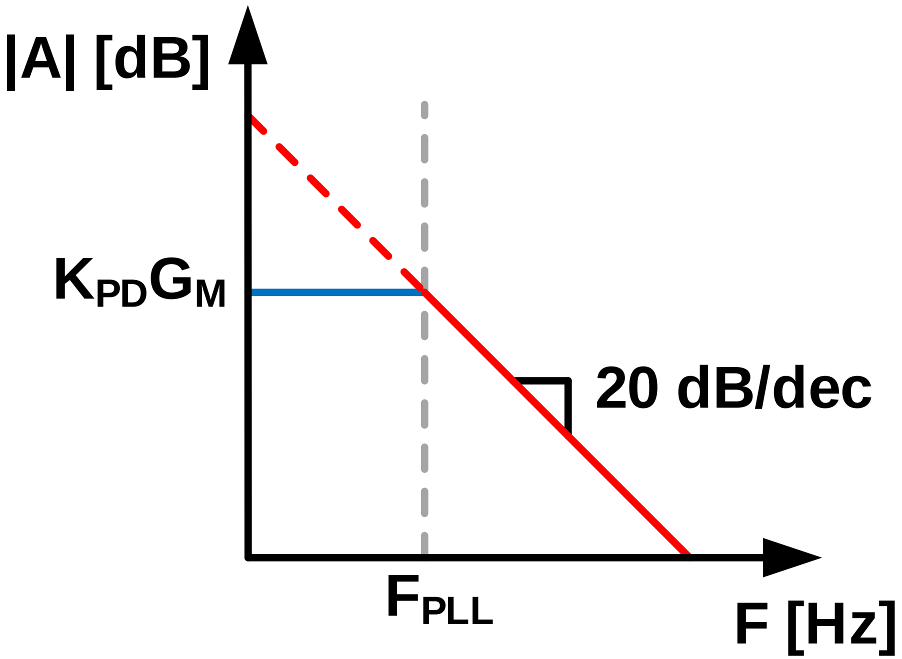
Generating V_B

- **Use a PLL to limit low-frequency response**

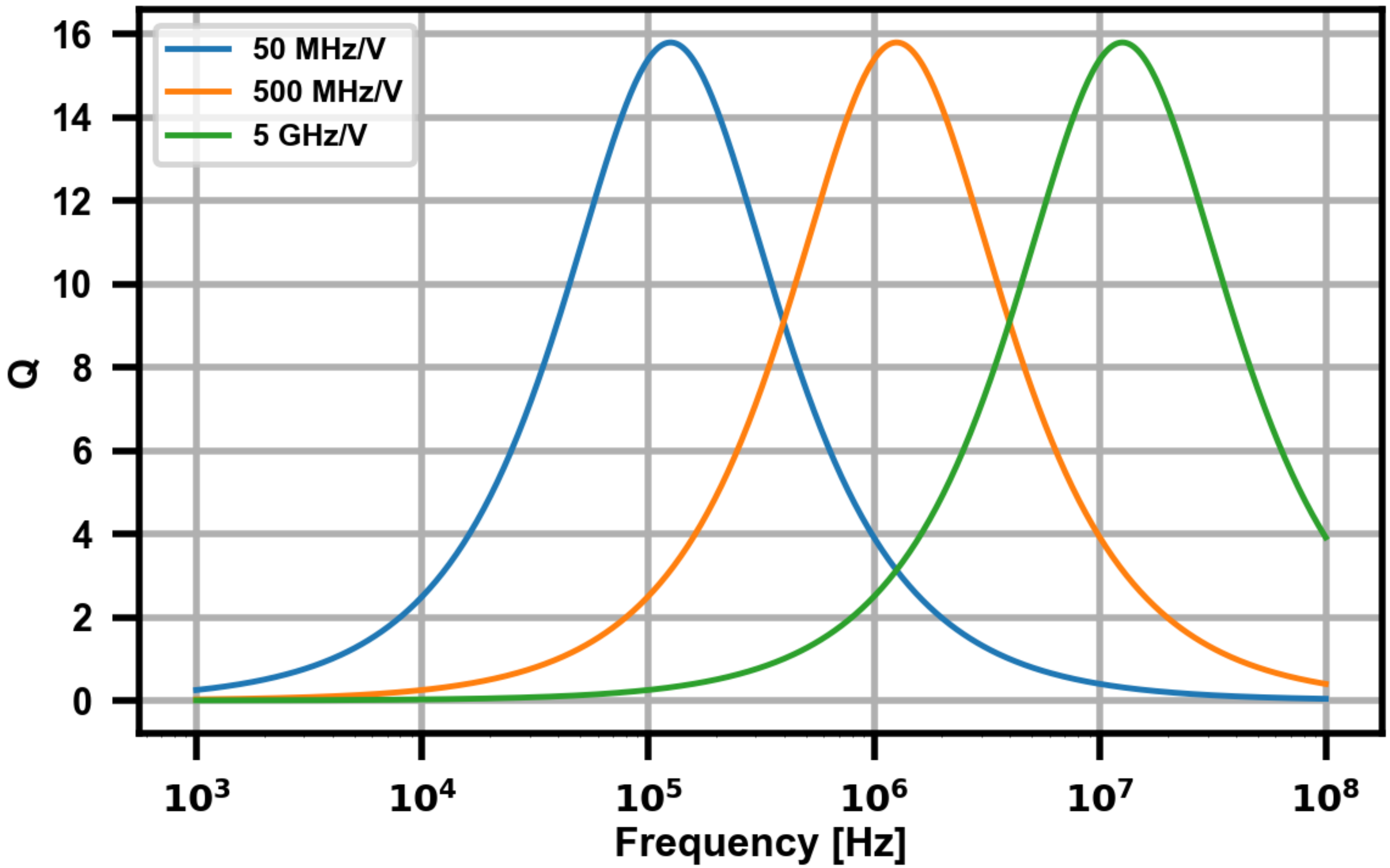


Generating V_B

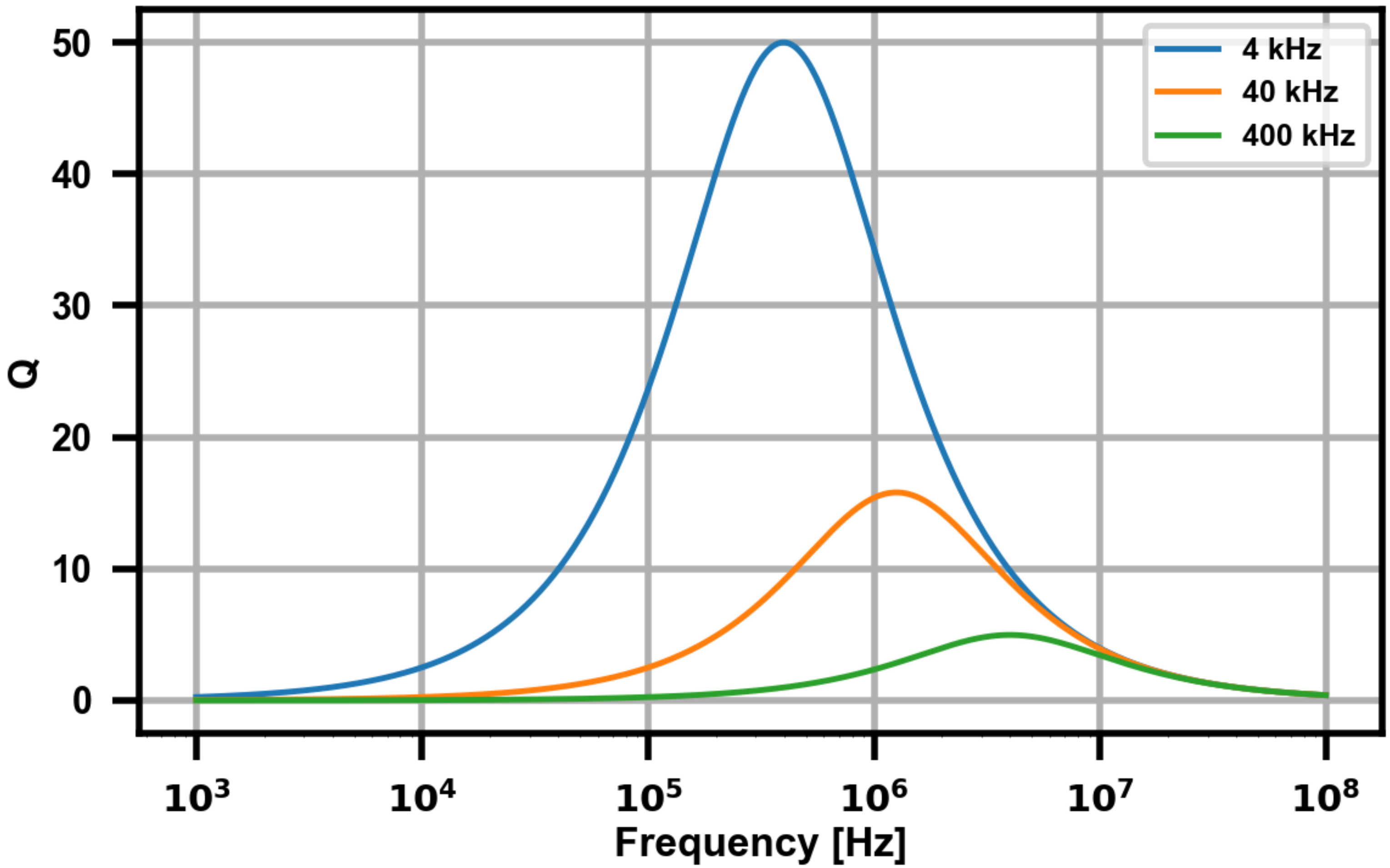




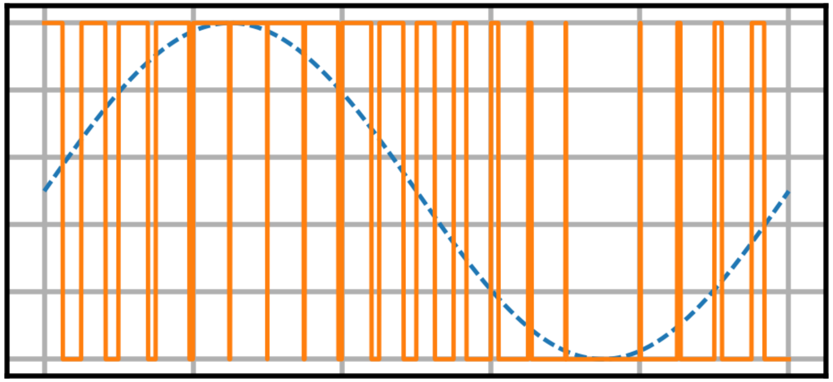
Inductor Q vs K_{VCO}

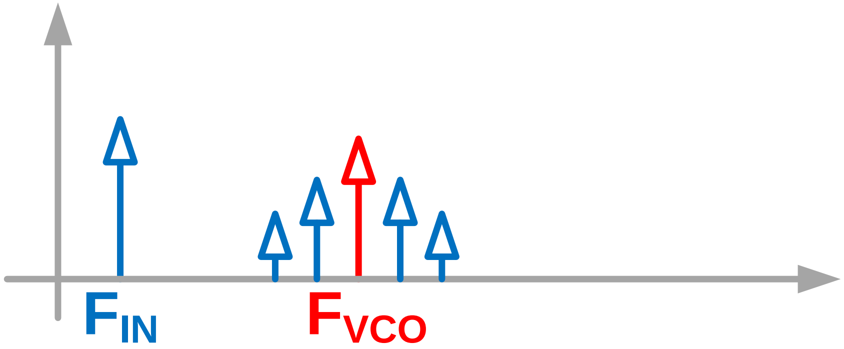


Inductor Q vs PLL Bandwidth

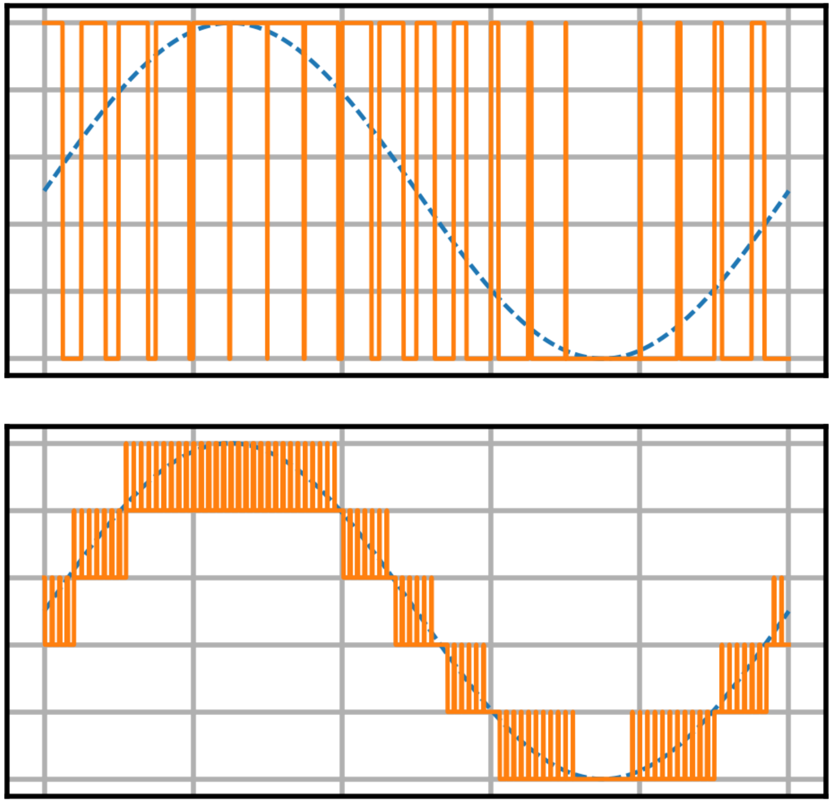


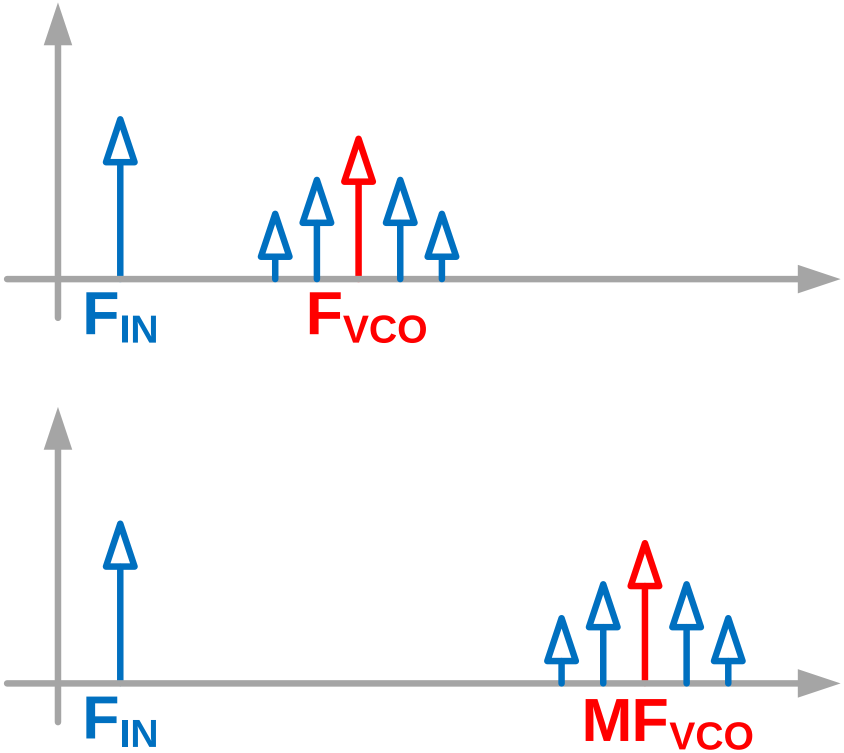
Mitigating PWM Tones





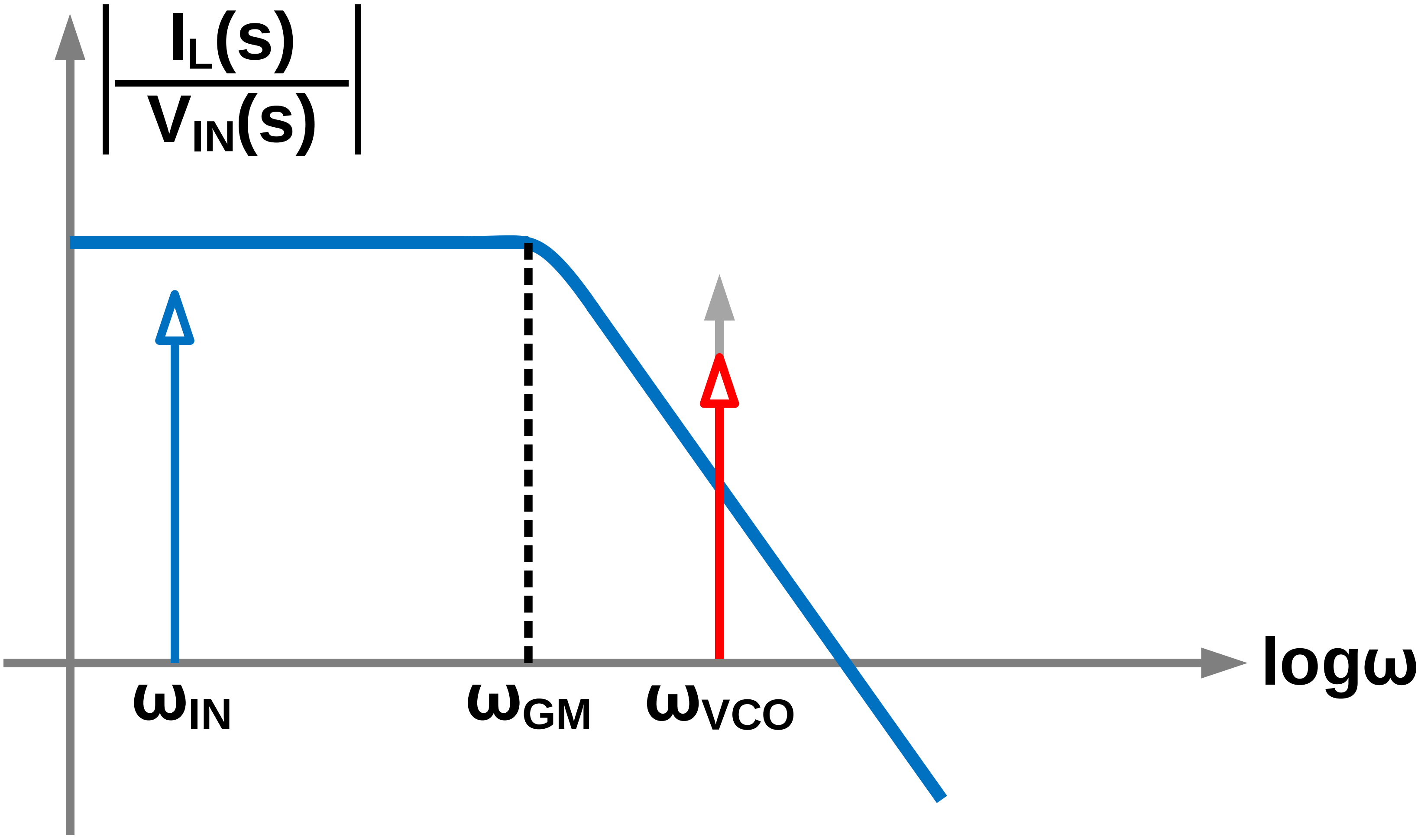
Mitigating PWM Tones



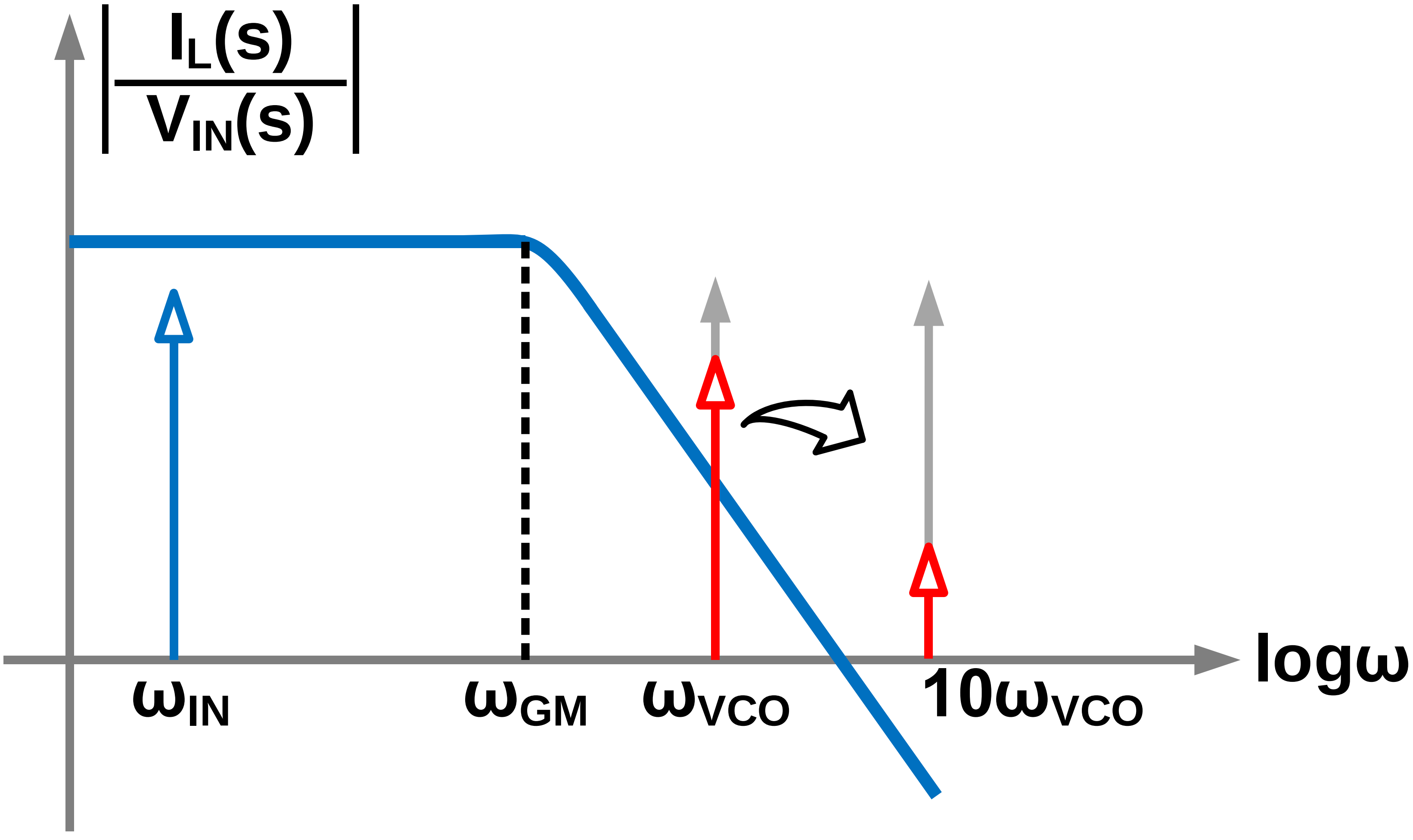


- **PWM tones move to MF_{VCO}**

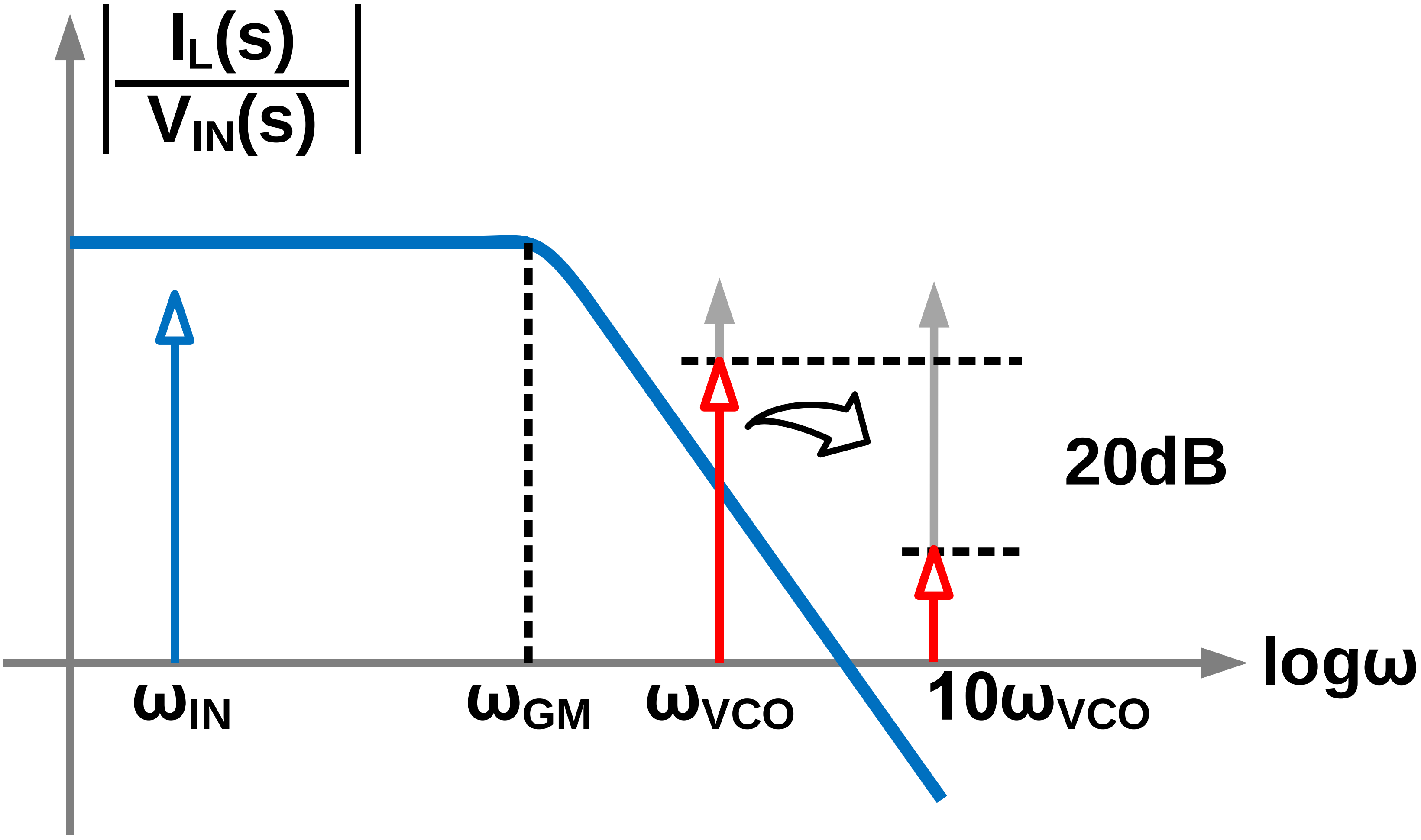
Reducing Spurious Tones



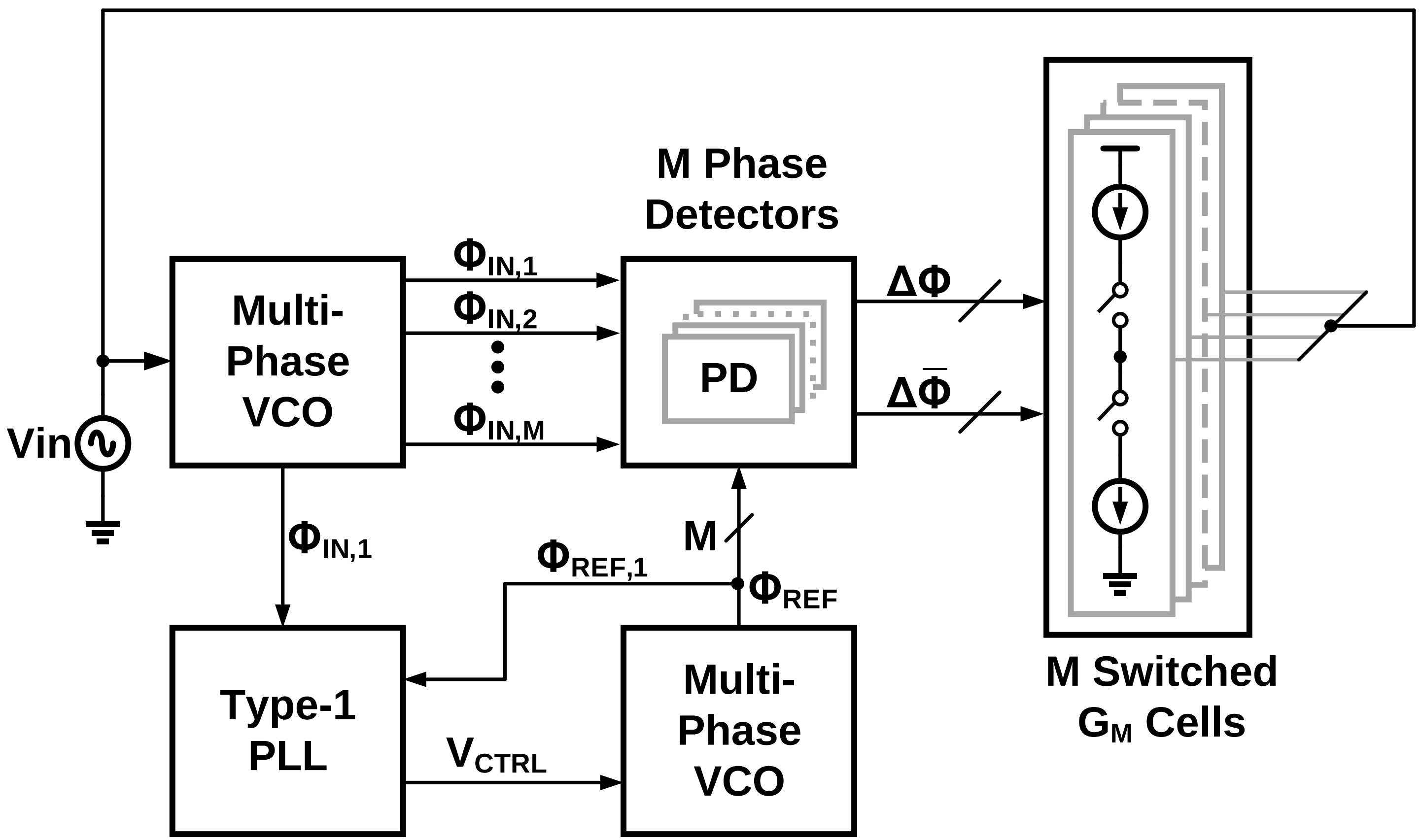
Reducing Spurious Tones



Reducing Spurious Tones



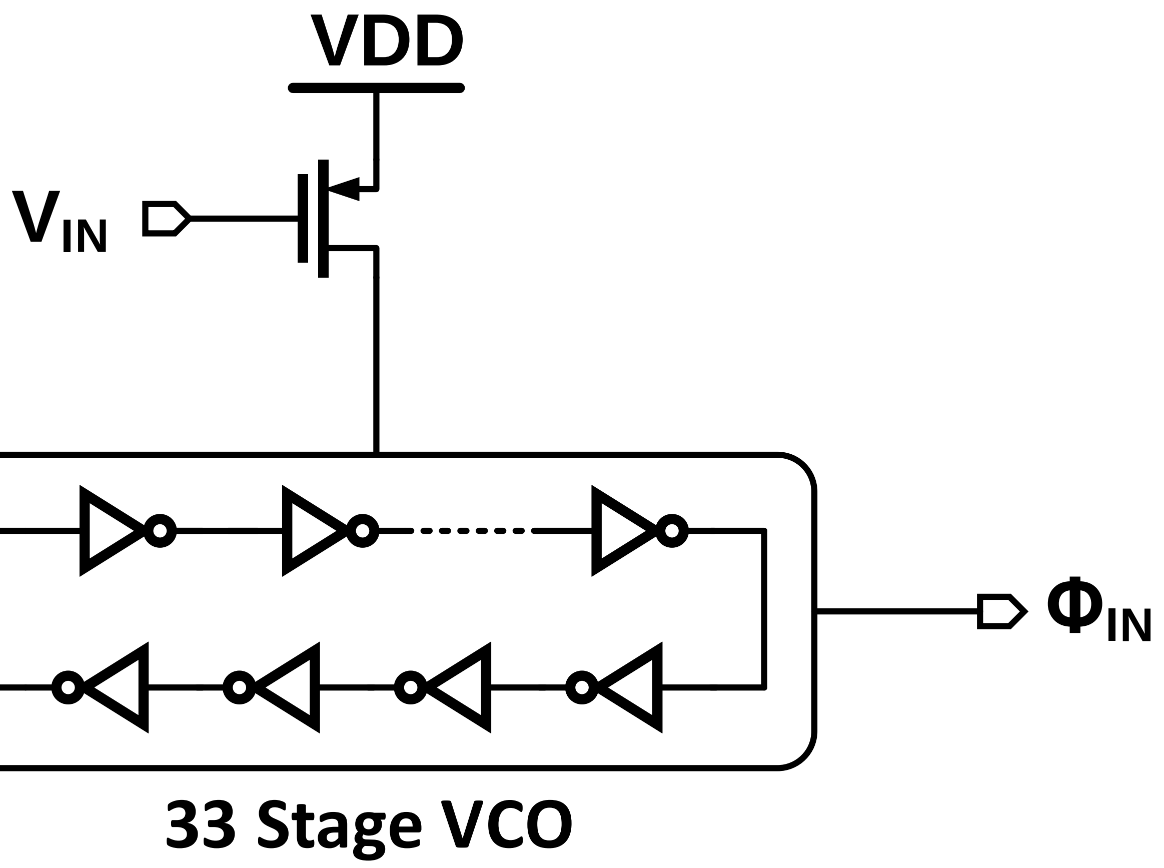
Complete Architecture



$$L = \frac{1}{K_{VCO} K_{PD} G_M M}$$

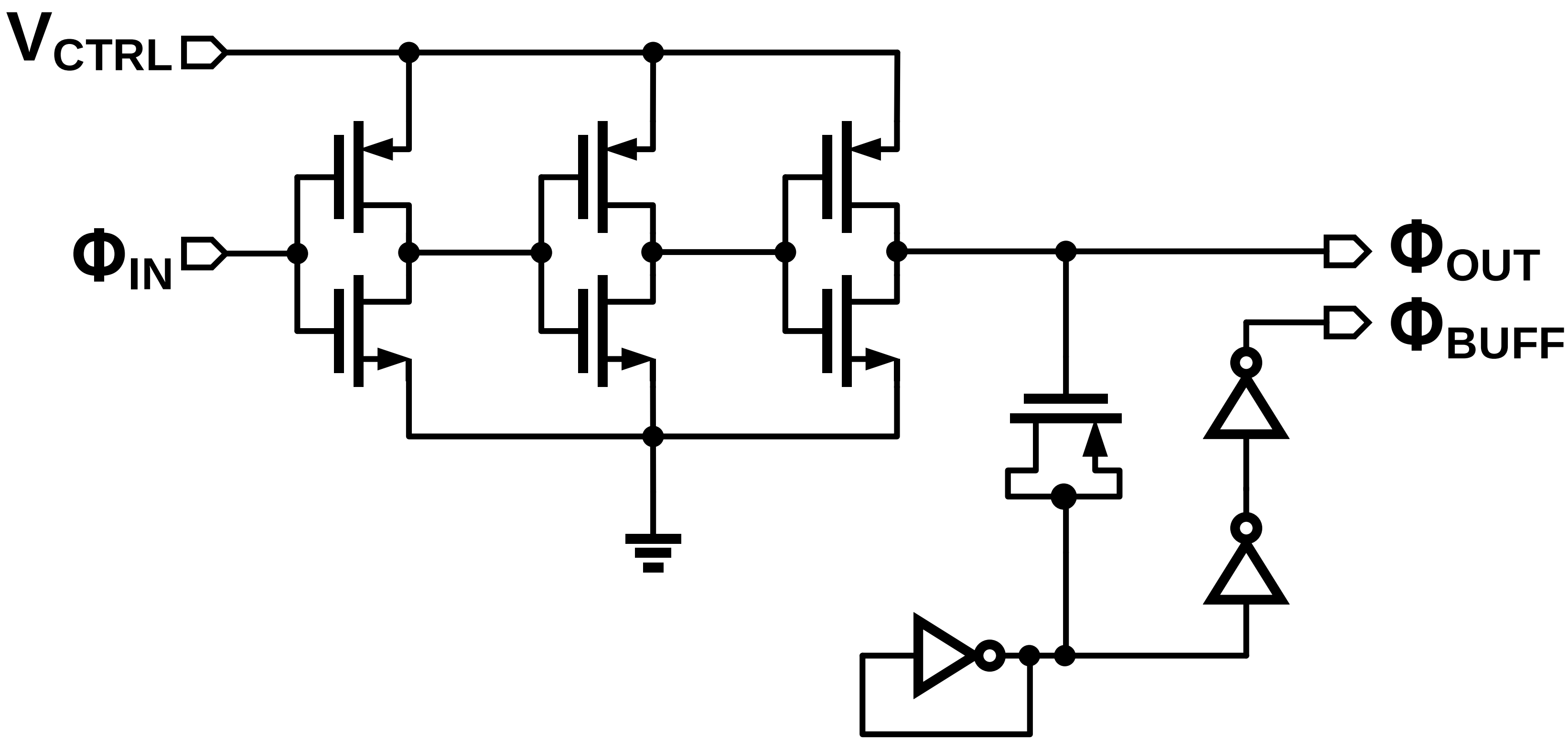
Voltage-Controlled Oscillator

- **Each delay cell is an inverter**
- **Biasing controlled by current-limiting PMOS**



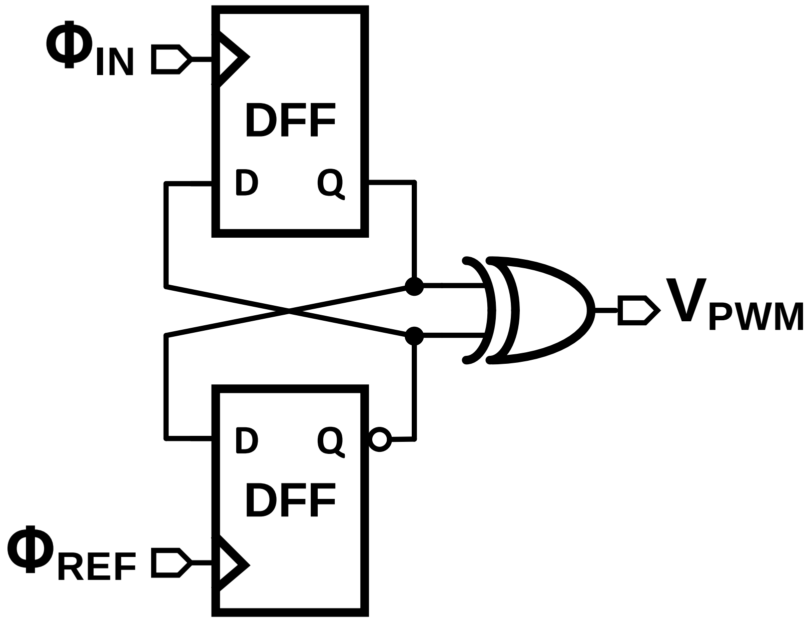
Delay Cell

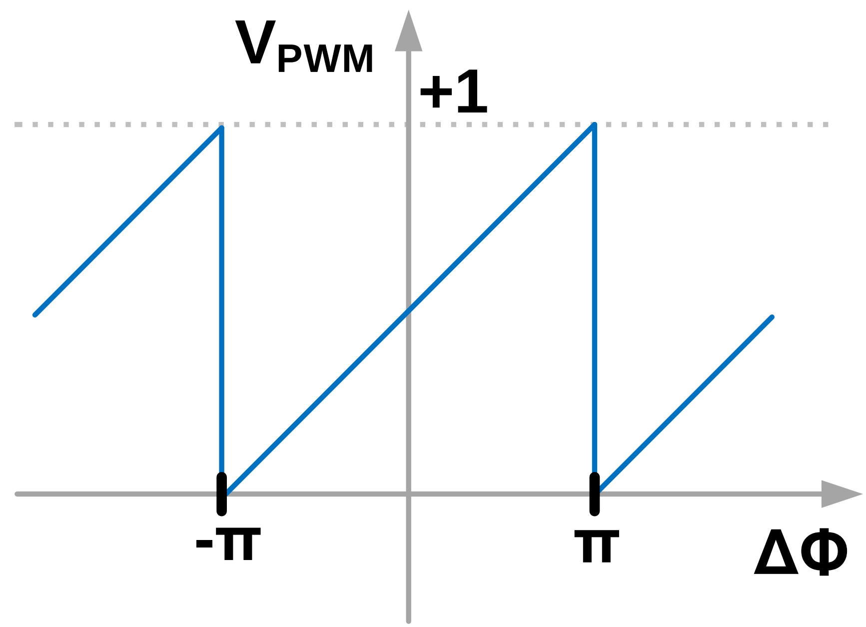
- **Need to bring output phase to full scale**



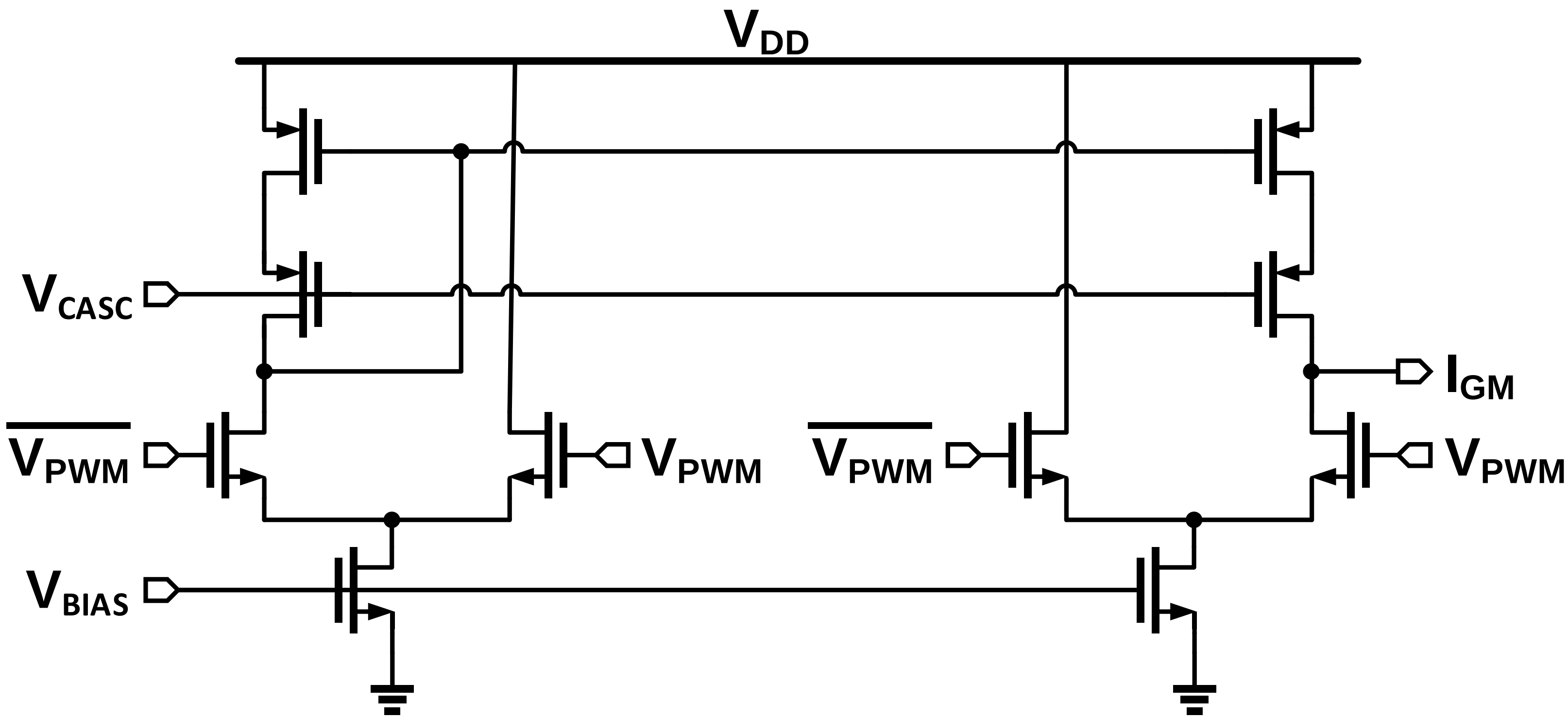
Phase Detector

- Two-state PD gives K_{PD} = 1/2π V/rad



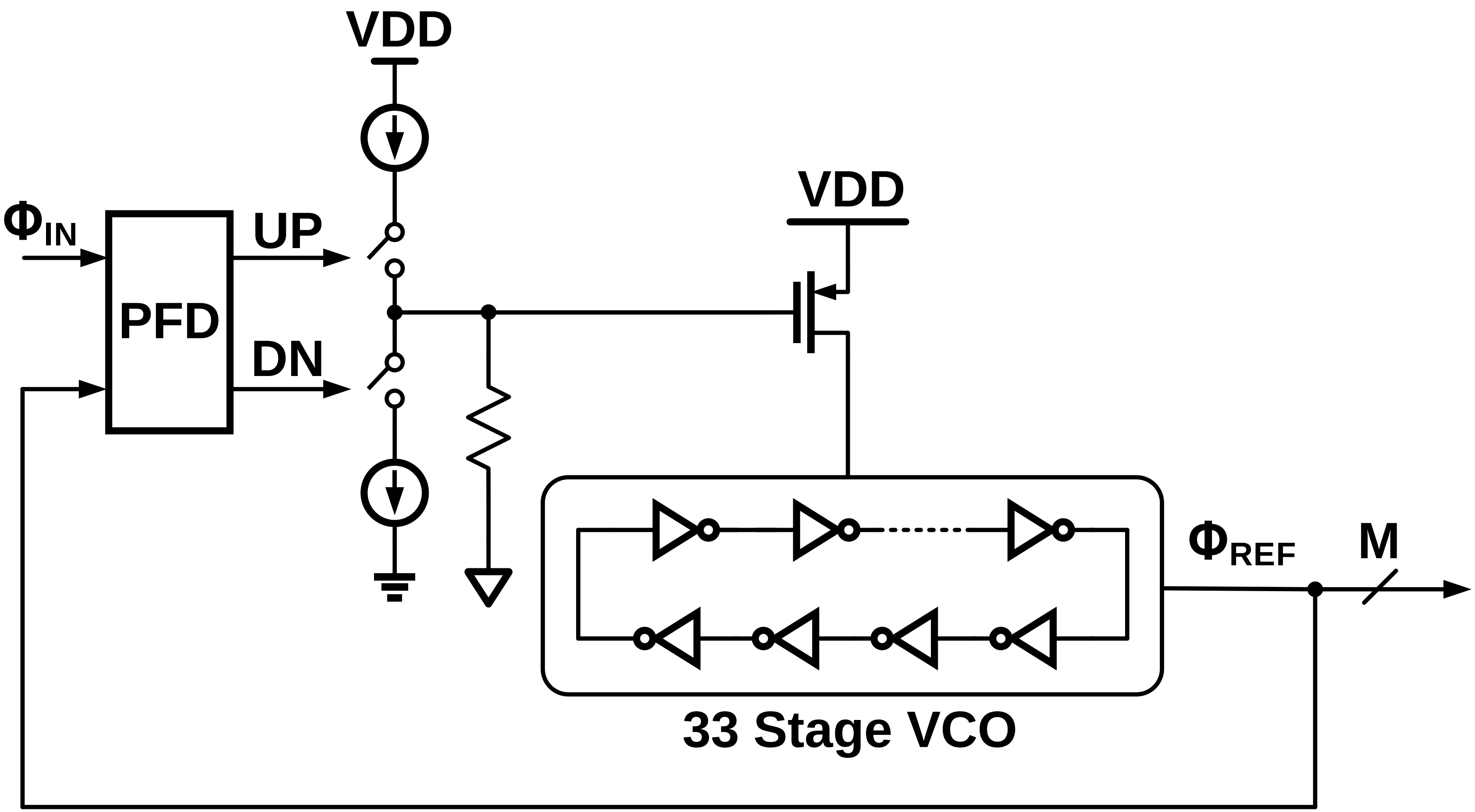


Switched G_M Cell



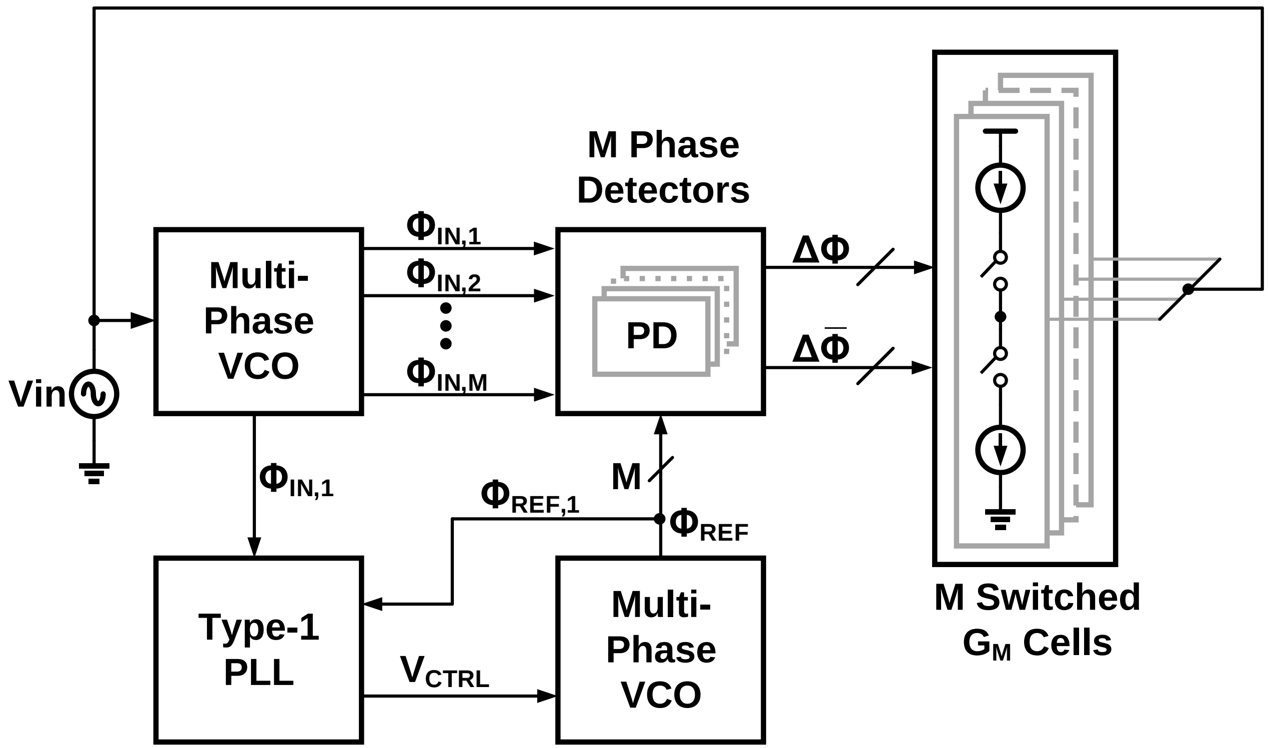
- Mirror G_M used to match currents
- Diff pairs prevent transient discontinuities

Type-I PLL



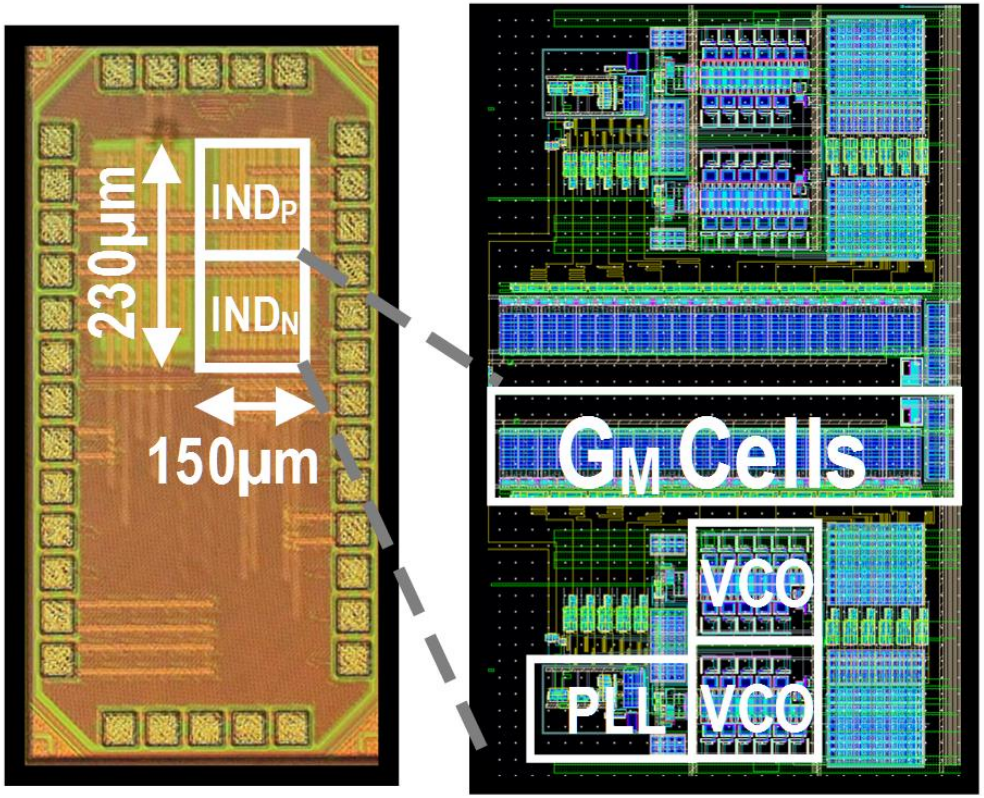
Design Specifications

- K_{VCO} tunable from 50 MHz/V – 500 MHz/V
- G_M tunable from 10 µA – 50 µA / cell
- L tunable from 150 µH – 1.5 mH



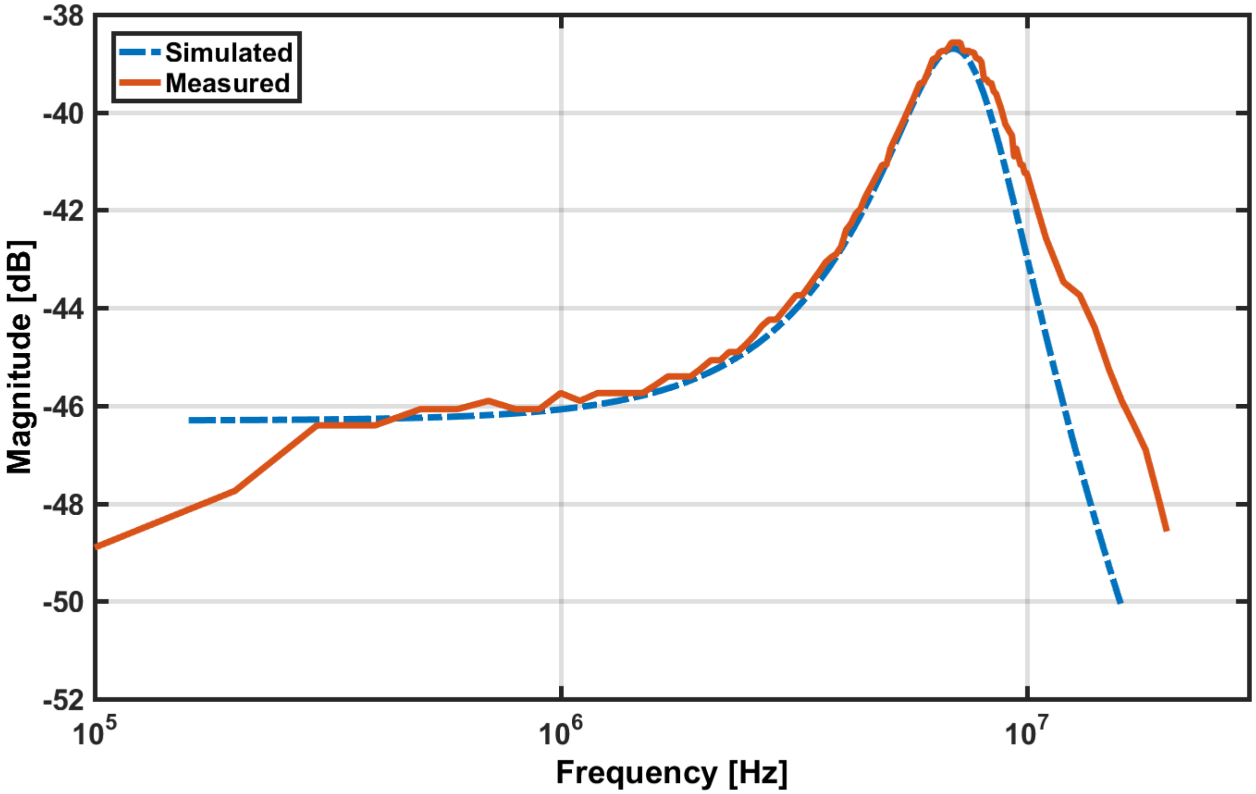
Die Photo

- **Fabricated in TSMC 65nm CMOS**
- **Inductor occupies 0.017 mm² area**



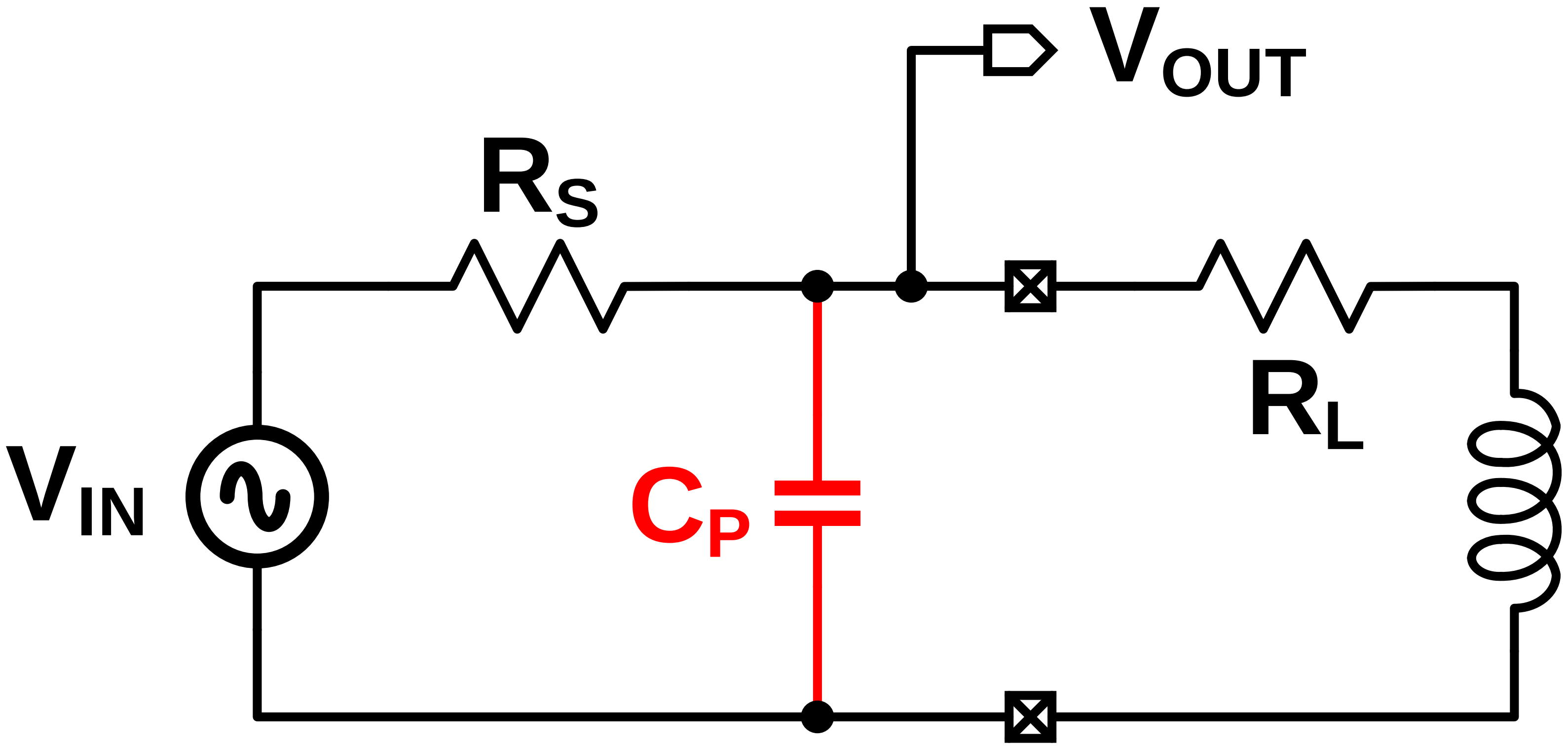
Measurements

- **Tested inductor in PCB passive filter**
- **Consumes 528µW of power**



Test Schematic

- Results limited by parasitic capacitance



Summary

- **Time-based inductor achieves significant area reduction**
- **Highly digital design scales with process**
- **Inductance value easily tunable**

Acknowledgements

- **Analog Devices Inc. for financial support**

- **BDA for providing Analog Fast Spice (AFS) simulator**